Two-Sample PLL with Harmonic Filtering Capability Applicable to Single-Phase Grid-Connected Converters

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Abstract— The two-sample phase locked loop (2S PLL) in single-phase digitally-controlled grid-connected power converters provide synchronization with a minimal computational burden. However, the distortion of the grid voltage deteriorates the performance of the 2S quadrature signal generator. To solve this issue, this paper introduces a harmonic filtering (HF) structure based on observers of the input voltage for the fundamental and selected harmonics. The stability and sensitivity of the 2S PLL with HF is analyzed. In comparison with SOGI based HF, the observers provide a narrower band pass and the subsequent deterioration of the response time is compensated by adapting the filter gains dynamically. The results obtained, both in simulation and experimentally, validate the proposal and compare its performance with other widely adopted PLLs providing harmonic rejection capability. The computational burden is analyzed and in the case of the proposals depends on the number of observers and the use or not of the adaptive strategy based on steepest descent.

I. INTRODUCTION

With the increasing penetration of grid-connected power converters, the requirements imposed by international standards and grid codes to their operation as frontends for both distributed energy resources (DER) and loads have increased. Among other functionalities, controllers in power converters must consider their effects on the local grid and contribute to the proper operation of the overall power system, i.e. by adjusting the power factor [1] and the dynamic response [2], which becomes more challenging in the case of disturbances and transients [3], [4]. One of the key elements to perform these tasks is the synchronization subsystem, which must be able to track the grid voltage at the converter connection point and maintain that synchronization even while electrical disturbances occur.

Digital controllers in grid-connected power converters use either open-loop [5]–[7] or closed-loop [8] strategies to achieve the grid synchronization. In the case of single-phase

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grid-connected converters, the zero-crossing detection is a simple open-loop synchronization method, but very sensitive to the harmonic distortion and phase noise [9]. In such operation conditions, a closed-loop synchronization system is preferred and the PLL is commonly used [10]–[12] to track the phase of the fundamental component of the grid voltage. The phase detector (PD) and the loop filter (LF) must reject the harmonic components, which is more difficult in the case of single-phase PLLs based on the Park transform as the PD requires a quadrature signal generator (QSG), and the presence of harmonic distortion and frequency variations may deteriorate its performance. From the point of view of the PLL structure, different strategies focused on the modification of the QSG have been proposed to address these issues, as reported in [13]. The most significant being the concept of Delayed Signal Cancellation (DSC) [14]–[23] and moving average filters (MAFs) [21]–[24]. The strategies proposed for the harmonic elimination in the synchronously rotating reference frame (SRF) can also be classified in open- and closed-loop. The open-loop methods cover proposals based on DSC, MAF, second order generalized integrators (SOGIs) [25]–[29], filtering [30]–[32], pre-processed algorithms [32], fast Fourier transform (FFT) [33], sliding discrete Fourier transform (SDFT) [34], recursive discrete Fourier transform (RDFT) [35]–[37] and sliding-Goertzel-transform [38], [39]. Considering the harmonic elimination precision, these strategies may present large error if the grid contains other disturbances not contemplated in the design, such as grid frequency variation. This issue is overcome by adopting a closed-loop strategy based on multi-harmonic decoupling cell (MDC) and multi-harmonic SRF filtering (MSF) [39]. Enhanced structures [40], notch type adaptive filters [41], [42], observers of the frequencies of interest are proposed in the rotating reference frame (RRF) [43] and in the SRF [44] or selective harmonics elimination (SHE) methods [45], [46].

Following this line of achieving enough accuracy and low computational burden PLLs based on the Park transform, the 2S PLL, presented in [47], has a QSG that only requires a buffer for two samples (Fig. 1). This QSG considers a restricted frequency variation of the line voltage around the central frequency and utilizes the signal variation within three consecutive sampling periods to generate the in-quadrature signal. A drawback of this approach is the low immunity to voltage harmonic distortion. The digital implementation of the 2S PLL proposed in [48] is aimed at minimizing the

computational burden of the 2S PLL for implementation in a field-programmable gate array (FPGA) but it does not improve its harmonic filtering capability.

Since the sensitivity to the voltage harmonic distortion is a handicap in the 2S PLL, this paper proposes to include an adaptive filter structure with minimal computational burden. The proposal is based on disturbance observers tuned at the frequency components of interest (up to the seventh harmonic) and using a closed-loop structure. The operating principles of the proposed filtering strategy and the assessment of its computational burden are also provided in this paper. Finally, the proposal is evaluated with simulations and experimentally. The paper is organized as follows. Section II compares the architecture of the proposed 2S PLL with adaptive harmonic filtering capacity. In Section III, the performance of the proposed PLL is compared with the SOGI PLL by simulation, while in Section IV, the comparison is carried out experimentally. In both sections, harmonically distorted grid voltages and fundamental frequency variations. Conclusions evaluating the applicability of the proposal to bidirectional H-bridge are finally provided.

II. 2S PLL WITH ADAPTIVE HARMONIC FILTERING CAPACITY

In order to filter out the voltage harmonic distortion, an adaptive filtering structure is proposed, as shown in Fig. 1. Each block H_i constitutes an observer of each ith frequency component of interest in the grid voltage, i.e. fundamental plus 3rd to 7th odd harmonics and, the observed i^{th} component at the sampling interval k, $o_{i,k}$, is, then, estimated from the error signal, e_k. The contribution of each observer H_i to minimizing e_k is balanced through the gains K_i. By zeroing the error signal e_k, the values $\alpha_{i,k}$ are estimated and $\alpha_{1,k}$ is used as the PLL input, which makes the proposed filtering structure useful to other QSGs than the 2S.

From Fig. 1, the obtained closed-loop equation is

$$\frac{e(z)}{v(z)} = \frac{1}{1 + \sum_{i=1}^{\text{max. order}} K_i H_i(z)} \tag{1}$$

the summation collects the contribution of the fundamental and all the harmonic components relevant for filtering purposes. From (1), each observer H_i has to result in a resonance at the ith frequency, which nulls e_k in steady state.

Moreover, the transfer function H_i relates the scaled signal of the grid voltage at the frequency of interest, $o_{i,k}$, and the overall error signal due to the set of observers, e_k, and, if the error signal is zero, each product $K_i H_i$ tracks the ith frequency component of the grid voltage without error. To achieve this, a high gain, without phase displacement, is required. Moreover, to avoid interferences between observers, each observer must exhibit a relatively low gain at frequency orders different than i, and, then, the following configuration is proposed for H_i

$$H_i(z^{-1}) = \frac{o_i(z^{-1})}{e(z^{-1})} = \frac{H_i'(z^{-1})}{1 - H_i'(z^{-1})} \tag{2}$$

where $H'_i(z^{-1})$ estimates the current value of the ith component from the previous samples. In order to evaluate $H'_i(z^{-1})$, the

phasorial representation of the ith component in a stationary reference frame at the sampling interval k is considered:

$$\alpha_{i,k} = A_{i,k} \cos(i\omega T_s k) + \alpha_{i,0} \tag{3}$$

$$\beta_{i,k} = A_{i,k} \sin(i\omega T_s k) + \beta_{i,0} \tag{4}$$

where, $A_{i,k}$ is the amplitude, ω is the fundamental frequency of the grid, and T_s is the sampling period. Then, and assuming that amplitude and grid frequency variations are slow enough, the estimated in-phase projection at instant $k+1$, $\alpha_{i,k+1}$, is obtained from

$$\alpha_{i,k+1} = \cos\left(i\frac{2\pi}{N}\right)\alpha_{i,k} - \sin\left(i\frac{2\pi}{N}\right)\beta_{i,k} \tag{5}$$

where $N = 2\pi/\omega T_s$ is provided by the PLL. Substituting (3) and (4), into (5) results in

$$\alpha_{i,k+1} = \frac{-\alpha_{i,k-2} + \alpha_{i,k}\left(4\cos^2\left(i\frac{2\pi}{N}\right) - 1\right)}{2\cos\left(i\frac{2\pi}{N}\right)} \tag{6}$$

that, in filter form, is rewritten as

$$G_i(z^{-1}) = \frac{\hat{\alpha}_i}{\alpha_i} = \frac{4\cos^2\left(i\frac{2\pi}{N}\right) - 1 - z^{-2}}{2\cos\left(i\frac{2\pi}{N}\right)} \tag{7}$$

where $\hat{\alpha}_i$ is the estimation of α_i and N is provided by the PLL. Then, with $H_i'(z^{-1}) = z^{-1}G_i(z^{-1})$ and using (2), $H_i(z^{-1})$ is obtained

$$H_i(z^{-1}) = \frac{N_i(z^{-1})}{D_i(z^{-1})} = \frac{z^{-1}G_i(z^{-1})}{1 - z^{-1}G_i(z^{-1})}$$
$$= \frac{\left(4\cos^2\left(i\frac{2\pi}{N}\right) - 1\right)z^{-1} - z^{-3}}{2\cos\left(i\frac{2\pi}{N}\right) - \left(4\cos^2\left(i\frac{2\pi}{N}\right) - 1\right)z^{-1} + z^{-3}}. \tag{8}$$

Figure 2.a shows the Bode diagram of H_1, according to (8), with three different T_s, where it is observed that the design requirements are accomplished and $|H_1(\omega_1)| \to \infty$. Other observers, at different sampling frequencies, perform similarly and result in $|H_i(\omega_i)| \to \infty$. Figure 2.b shows the equivalent Bode diagram of the SOGI (whose transfer function is H_{SOGI} which have a band-pass filter characteristic.

A. Adaptive Filter Gains

The filter gains are adjusted adaptively by means of a gradient descent method [49]. From the block diagram in Fig. 1, the instantaneous error of the HF is used to evaluate the continuous cost function, J, to be minimized. Then, in terms of the HF input signal and the contribution of each ith filter tap, which is adjusted through K_i, the cost function becomes

$$J(t) = \frac{e^2(t)}{2} = \frac{\left(v(t) - \sum_{i=1}^{\text{max. order}} K_i(t) o_i(t)\right)^2}{2}, \tag{9}$$

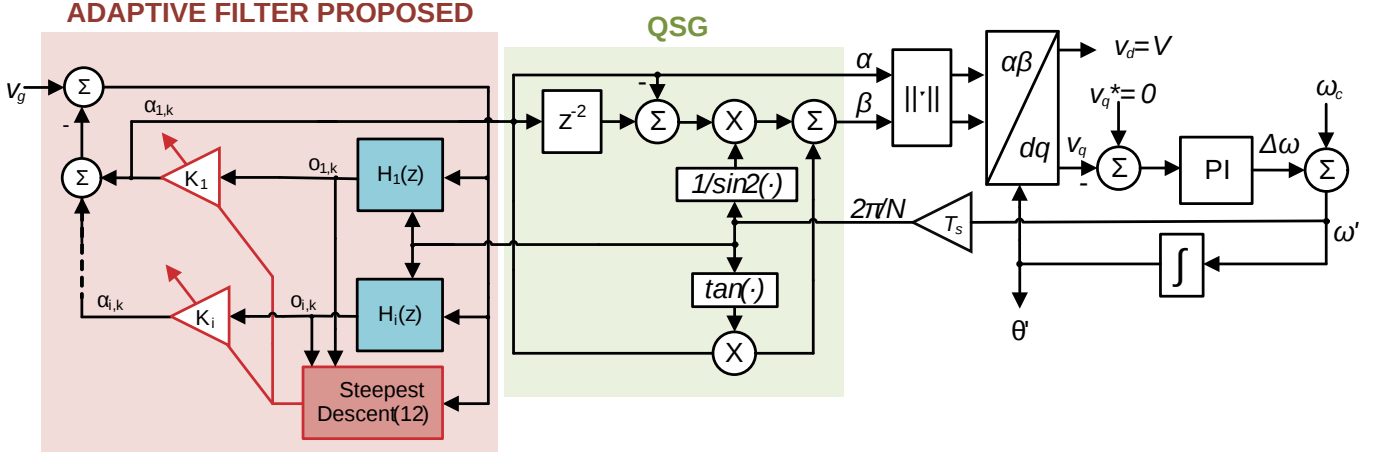where the contribution of each observer is considered. Then, the gains are adjusted by

Fig. 1: 2S-PLL in [47] including the proposed filter of the harmonic distortion of the grid voltage.
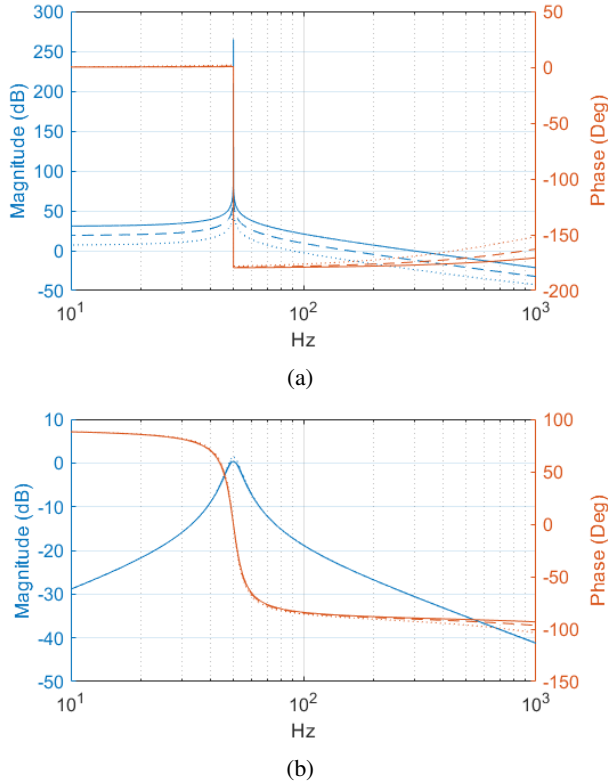

(a)

(b)

Fig. 2: Bode diagram of a) H_1 and b) H_{SOGI}. Continuous line: $T_s=2.e-5$ s, dashed line: $T_s=3.9e-5$ s, and dotted line: $T_s=7.8e-5$ s.

$$\frac{dK_i(t)}{dt} = -\eta \frac{\partial J}{\partial K_i} = \eta e(t) o_i(t), \qquad (10)$$

which is discretized as

$$K_{i,k} = K_{i,k+1} + \eta T_s e_k o_{i,k} \qquad (11)$$

where η is the learning rate and must be selected to balance the convergence rate and the steady-state error of the harmonic filter. More details about the procedure for selecting the most

appropriate η values can be found in [49]–[51]. From these considerations and (11), the selection of a suitable parameter η would depend on each product $e_k o_{i,k}$ and then, it is normalized here by means of resulting in the iterative rule

$$K_{i,k} = K_{i,k-1} + \mu \frac{e_k}{\sum_{i=1}^{\text{max. order}} o_{i,k}^2} o_{i,k} \qquad (12)$$

where $\eta T_s = \frac{\mu}{\sum_{i=1}^{\text{max. order}} o_{i,k}^2}$ and $\mu \in R^+$ and is selected to ensure the filter stability and convergence.

Since the performance of gradient descent methods can be sensitive to the initial conditions [51], [52], an initial guess for each K_i considers that the filter error in (1) equals zero for the selected frequency components. That is, $|H_i(\omega_i)| \to \infty$ forces that the contribution of each ith component results in null error.

As an example, let's consider the fundamental plus the 3rd and 5th harmonics. Then, the structure in Fig. 1, without gain adaptation, is reduced to the scheme shown in Fig. 3, with $K_{1,0}$, $K_{3,0}$ and $K_{5,0}$ as filter gains. The resonant sections in H_3 and H_5, within the 3rd and 5th inner loops, must cancel the voltage harmonic distortion at these frequencies. Simultaneously, other control targets of the control loops are *i)* minimize the attenuation below the resonant frequency and *ii)* minimize the deviation of the relative harmonic phase. $K_{3,0}$, and $K_{5,0}$ must be increased to achieve *i)* while, for *ii)*, $K_{3,0}$, and $K_{5,0}$ must decrease. The tuning procedure starts with the inner loop, resulting in $K_{5,0}$ = 4.51e-3. Then, considering the closed loop transfer function T_5 = 1/(1+K_5H_5) and the next filtering stage, H_3, it results in $K_{3,0}$ = 2.73e-3. Finally, the value $K_{1,0}$ must compensate for the attenuation due to H_3 and H_5. By increasing $K_{1,0}$, the magnitude of the frequency response flattens at the fundamental but the resonance peaks, due to H_3 and H_5 and the DC component are not filtered out. Moreover, the time response becomes slower, so $K_{1,0}$ must be selected to achieve a fast-enough time response compatible with the required zero gain and zero phase at the fundamental. The constant, $K_{1,0}$ is selected as 6.79e-3. If frequency variations are likely to occur while starting the gain adaptation algorithm, a less restrictive approach must be adopted, and this value can
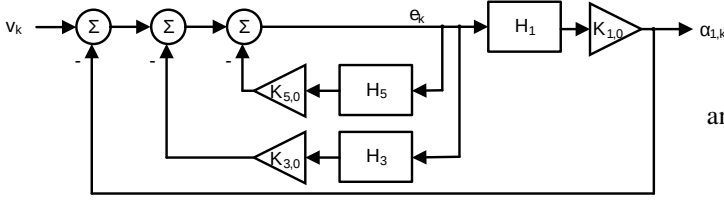
Fig. 3: Harmonic filtering structure for the fundamental plus the 3rd and 5th harmonics.

be increased to compensate for. Following the design example, other observers, at higher harmonic orders, can be included within the filtering structure.

B. Filter Stability

For simplicity sake, the filter stability is analyzed by considering two harmonic filter taps, at 3rd and 5th harmonics, but it can be extended to other sets of selected harmonics. The sampling frequency is large enough to ensure that variations of $N = 2\pi/\omega T_s$ around the central frequency of the PLL are limited and the ratio i/N is low enough. Moreover, the values K_i, despite of being dynamically updated in Fig. 1, are limited.

Then, the filter transfer function, $G_L(z^{-1})$, and the characteristic polynomial, $P_L(z^{-1})$, are defined as

$$G_L\left(z^{-1}\right) = \frac{\alpha_1\left(z^{-1}\right)}{v\left(z^{-1}\right)} = \frac{K_1 H_1\left(z^{-1}\right)}{1 + \sum_{i=\{1,3,5\}} K_i H_i\left(z^{-1}\right)} \quad (13)$$

and

$$P_L\left(z^{-1}\right) = 1 + \sum_{i=\{1,3,5\}} K_i H_i\left(z^{-1}\right) = 0 \quad (14)$$

By applying the Jury criterion, the following necessary conditions are achieved, which are valid under the assumption i/N small enough:

$$\sum_{i=\{1,3,5\}} n_i^6 K_i > 0 \quad (15)$$

$$2 > \sum_{i=\{1,3,5\}} K_i \quad (16)$$

The first condition is accomplished by using $K_i \in R^+$, and, from the second one, $K_i \in (0,2)$, independently of the selected harmonic orders. The initial values given in Section II.A verify this condition.

C. Sensitivity to N

The sensitivity of the closed loop transfer function $T(s,N)$ to N parameter variations are evaluated by

$$S_{N_k}^T\left(s, N_k\right) = \frac{\partial T\left(s, N\right)}{\partial N} \frac{N}{T\left(s, N\right)} \quad (17)$$

where

$$T = \frac{K_1 H_1\left(s, N\right)}{1 + K_1 H_1\left(s, N\right) + \sum_i^n K_i H_i\left(s, N\right)} \quad (18)$$

and, using $z = e^{sT_s}$ within (7):

$$H_i\left(s, N\right) = \frac{a_i e^{2T_s s} - 1}{b_i e^{3T_s s} - a_i e^{2T_s s} + 1} \quad (19)$$

which results in (20).

If T_s is small enough for the selected maximum harmonic order of the filter, then the following approximations can be used.

$$b_i \approx 2, \; a_i \approx 3, \; \frac{\partial b_i}{\partial N} \approx \frac{8\pi^2}{N^3} i^2, \; \frac{\partial a_i}{\partial N} \approx \frac{32\pi^2}{N^3} i^2 \quad (21)$$

and, then,

$$\frac{\partial H_i\left(s, N\right)}{\partial N} \approx \frac{8\pi^2 i^2}{N^3} e^{3T_s s} \frac{5e^{2T_s s} + 1}{\left(b_i e^{3T_s s} - a_i e^{2T_s s} + 1\right)^2} \quad (22)$$

resulting in

$$S_N^T\left(s, N\right) \approx \frac{8\pi^2}{N^2} e^{3T_s s} \frac{\left(5e^{2T_s s} + 1\right)}{\left(3e^{2T_s s} - 1\right)} \cdot$$
$$\cdot \frac{1 + \frac{\left(3e^{2T_s s} - 1\right)}{\left(2e^{3T_s s} - 3e^{2T_s s} + 1\right)} \sum_i^n K_i\left(1 - i^2\right)}{\left(2e^{3T_s s} - 3e^{2T_s s} + 1\right) + \left(3e^{2T_s s} - 1\right)\sum_i^n K_i} \quad (23)$$

where, considering a certain set of harmonic orders and limiting the applied K_i values to maintain the stability (see Section II.B), the sensitivity of the closed loop transfer function to the parameter N is $S_N^T\left(s, N\right) \propto \frac{1}{N^2}$ and, hence, $S_N^T\left(s, N\right) \propto \left(\omega' T_s\right)^2$, which can be kept low enough by selecting the proper harmonic orders and the sampling frequency used.

III. SIMULATION RESULTS

The proposed harmonic filter (HF) stages, considering 3rd, 5th and 7th voltage harmonics (H_1 plus H_3, H_5 and H_7 blocks), using both versions, the non-adaptive ($\mu=0$ and $K_1=1.98e-3$, $K_3=1.51e-4$, $K_5=3.9e-4$, $K_7=3.74e-4$) and adaptive (relatively slow, $\mu=5e-5$, and relatively fast, $\mu=5e-3$), have been incorporated to the 2S PLL and evaluated by means of a Monte Carlo (MC) tests using Matlab/Simulink®. While focusing on evaluating the harmonic rejection capability provided to the 2S PLL, a performance comparison with widely adopted PLLs providing harmonic rejection capability is also given: the same tests and conditions have been run with the 2S PLL without prefiltering stage [47], the SOGI PLL [4], [51], with crossover frequency set to $1.8\ Hz$, the Multi SOGI (MSOGI) PLL [52], with SOGIs at the fundamental, 3rd, 5th and 7th, the DSC PLL [53], with rotations at $2\pi/8$, $2\pi/16$ and $2\pi/32$ radians, and the MAF PLL [54] with constant window length equal to one grid period at the nominal grid frequency. The same phase detector, loop filter ($T_{settling}=0.6\ s$ [4]) and oscillator are used in all the cases. The sampling time, T_s, is $156.25\ \mu s$.

All the MC tests consider harmonically distorted grid voltages, within the limits stablished in EN 50160 [55],

$$S_N^T (s, N) = N \frac{\frac{\partial H_1(s,N)}{\partial N} + \frac{\partial H_1(s,N)}{\partial N} \sum_i^n K_i H_i - H_1 \sum_i^n K_i \frac{\partial H_i(s,N)}{\partial N}}{H_1 \left(1 + K_1 H_1 (s, N) + \sum_i^n K_i H_i (s, N)\right)} \quad (20)$$

interharmonics and other effects due to the measure chain, such as noise and DC components. A total of 171 simulation conditions are generated through Latin Hypercube Sampling (LHS), which allows the representative number of MC tests to be reduced. Voltage harmonic combinations, with orders from 2nd to 50th and amplitudes within the individual and collective limits in EN 50160 (*VTHD $\leq$ 8 %*), are considered. Results are presented according to a uniform probability density function (PDF). The nominal grid frequency changes in the test following a normal PDF, according the EN 50160 limits. The interharmonics within DC and $100\ Hz$ are also included in the LHS by means of a uniform PDF and individual peak value of the nominal grid voltage equal to *0.5 %* .

The resulting PDFs for the measured mean phase error ($\overline{\theta_e}$) in steady state are shown in Fig. 4.a. The PLLs which result in the best medians are DSC and MAF PLLs, with *0.395^o* and *2.004^o*, respectively, followed by SOGI and MSOGI PLLs, with medians equal to *2.044^o* and *2.045^o*, respectively. The 2S based PLLs result in the worst medians, *2.704^o* for the 2S PLL without harmonic filtering, and *2.810^o* to *2.821^o* for 2S PLLs with HF. However, in terms of variance and, hence, variability of performance, the worst variances correspond to 2S without HF, MAF and DSC PLLs, with *0.79^o*, *0.33^o* and *0.585^o*, respectively. The most consistent PLL, i.e. less variance, is the 2S PLL with slow adaptive HF (μ= 5e-5), resulting in 0.021^o. SOGI and MSOGI PLLs result in *0.024^o* and *0.023^o* variances respectively. Hence, the HF structure increases the performance consistency of the 2S PLL synchronization strategy (reduce the results variance) but the average error can increase up to *0.1^o*, depending on how fast the steepest descent algorithm operates on the filter gains. The measured phase error ripple ($\widehat{\theta_e}$) under the same steady-state test is shown in Fig. 4.b. The 2S PLL in [47] results in the worst phase ripple (median equals *0.618^o*) and harmonic filtering structures contribute to reduce this ripple to the range [*0.218^o*, *0.487^o*]. Other PLLs in the literature perform better, as shown in Fig. 4.b but it must be considered that only four, H_1, H_3 H_5 and H_7, filtering blocks have been used in the 2S PLLs with HF. If more blocks were included, despite of increasing the computational burden, this ripple (Fig. 4.b) and the average error (Fig. 4.a) would be further reduced. Within the set of widely adopted PLLs, the MSOGI shows the worst phase ripple results (the median is *0.128^o*). Best performers in terms of phase ripple are MAF and DSC PLLs, with 0.138^o and *0.139^o*, respectively.

The response to frequency ramps has also been evaluated through the steady-state MC conditions but including different starting phase angles, ramp magnitudes and lengths, assuming uniform PDFs and LHS to generate the test conditions, within the ranges [0°, 360°), [$-10\ Hz/s, 10\ Hz/s$] and [$20\ ms$, 500 ms], respectively. Figure 5.a and 5.b show the PDFs of the measured overshoots and response times to the frequency ramps. The dynamics of all the analyzed PLLs are dominated
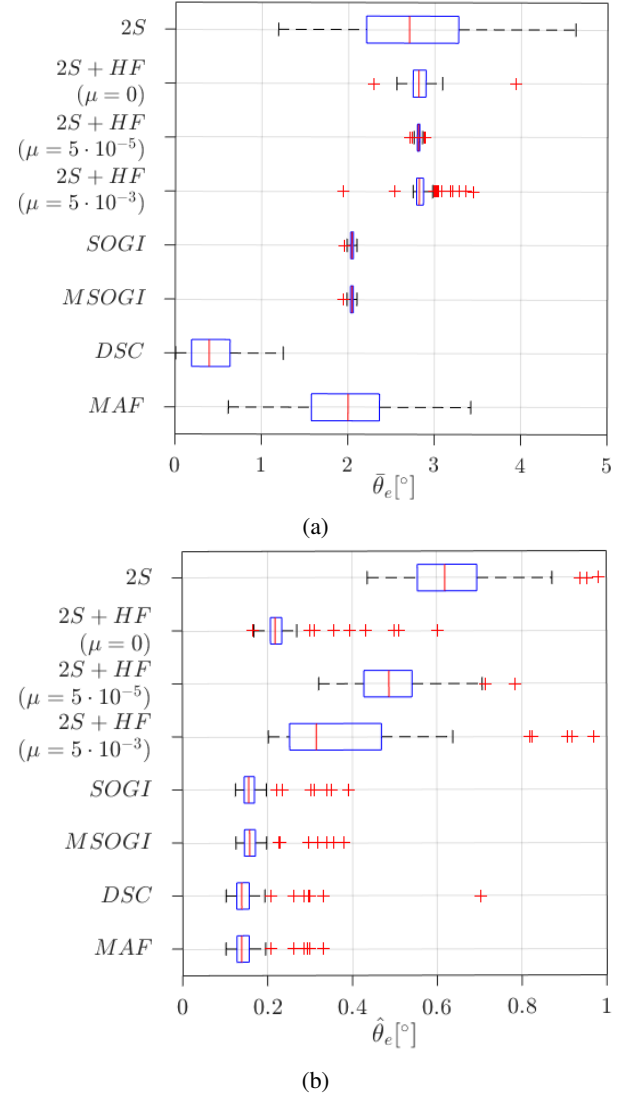

(a)

(b)

Fig. 4: Results of MC tests in steady state. Harmonic and interharmonic content, and the nominal grid frequnecy, are combined through LHS. a) Mean phase error and b) Ripple of the phase error.

by the inner filter loop and the effect of the HF stage is relatively low. The overshoots in Fig. 5.a, with medians in the range [39.058^o, 51.733^o] and variances in the range [25.205^o, 34.135^o], and the response times in Fig. 5.b, with medians in the range [348.75 ms, 467.969 ms] and variances in the range [249.147 ms, 416.721 ms], show that, overall, the 2S PLL without HF is the best performer in this dynamical test, despite of resulting in the worst steady-state performance. Among all the other evaluated PLLs, the best balance of overshoot and response time is due to the 2S PLL with slow adaptive HF.

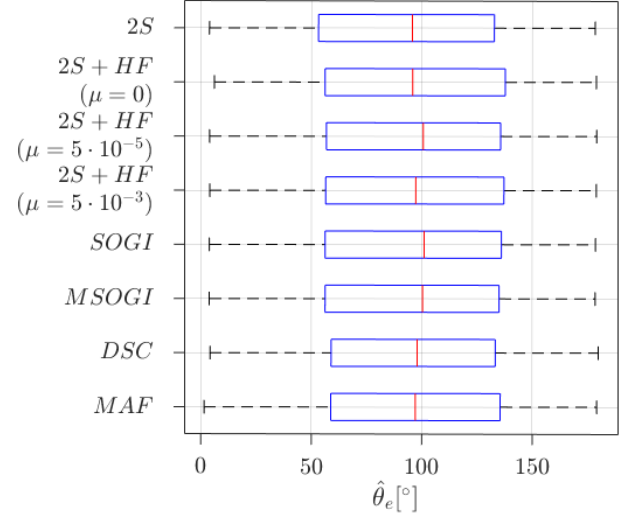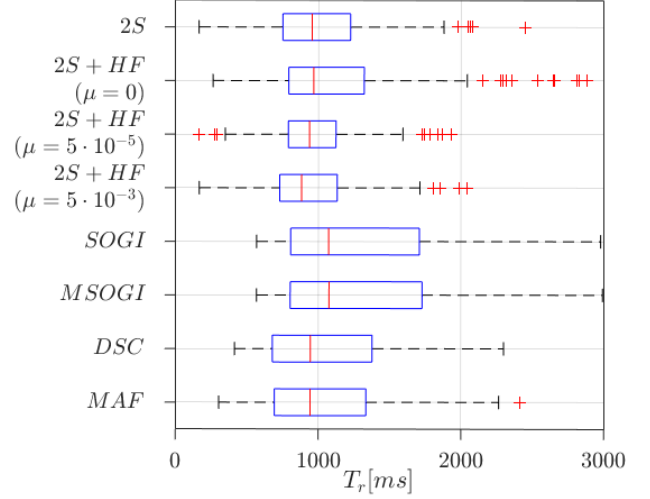The response to frequency jumps has been evaluated com-
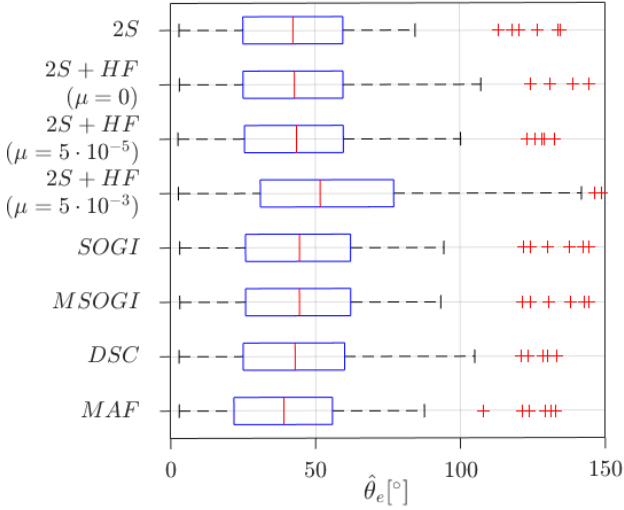
(a)
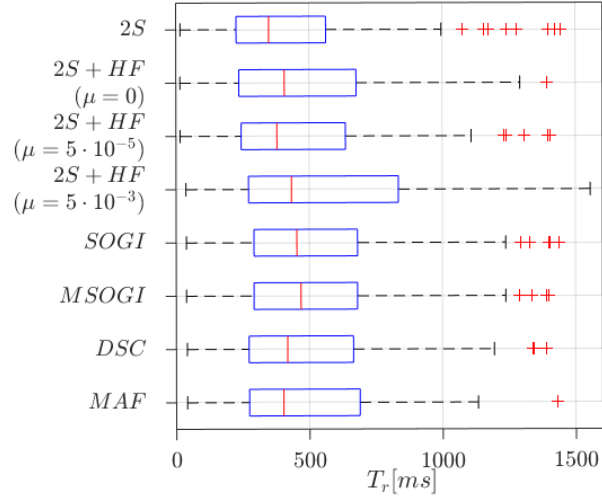
(b)

Fig. 5: Results of MC tests with frequency ramps. Starting phase angle, ramp magnitude and length are varied through LHS.

(a)

(b)

Fig. 6: Results of MC tests with frequency jumps. Starting phase angle and jump magnitude are varied through LHS.

bining the steady-state MC conditions with different starting phases and magnitudes, in the range $[0^o, 360^o)$ and $[-5\ Hz, 5\ Hz]$, and assuming uniform PDFs, and the results are shown in Fig. 6. All the analyzed PLLs result in similar overshoot PDFs (Fig. 6.a), with medians in the $[95.551^o, 100.985^o]$ range and variances within $[55.076^o, 60.430^o]$. The PDFs of the response times are shown in Fig. 6.b, where small performance differences are appreciated. In terms of response times, the best performer is the 2S PLL with fast $\mu = 5e-3$) adaptive HF, achieving $882.891ms$ and $298.721ms$ as median and variance, respectively. The worst performer is the MSOGI PLL (median and variance equal $1076.094ms$ and $684.313ms$, respectively). In comparison with frequency ramps, where the best performer 2S PLL is the slow adaptive version, sudden frequency changes are best managed by a more aggressive adaptive action.

Figure 7 shows the obtained results in the case of phase

jumps. The magnitude of the jumps is uniformly distributed in the range $[-90^o, +90^o]$ and the starting point is applied at different phase instants in the range $[0^o, 360^o)$. Again, LHS is used to combine these conditions with the steady-state test ones. The PDFs of the measured overshoots and response times in the phase errors after the transient are shown in Fig. 7.a and 7.b, respectively. The overshoots (Fig. 7.a) are similar for all the PLLs (medians within $[43.759^o, 44.748^o]$ and variances within $[33.159^o, 34.946^o]$) and the response times (Fig. 7.b) differ slightly. Within the 2S PLLs with HF, the fast adaptive version ($\mu = 5e-3$) shows the fastest median ($719.609ms$) but, as in the case of the slow adaptive version, both are less consistent than the non-adaptive HF. As in the case of frequency jumps, speeding up the steepest descent strategy, the PLL performs better. MSOGI and SOGI PLLs are the best performers in this test, achieving $589.688ms$ and $590.781ms$ medians, and $11.293ms$ and $10.656ms$ variances, respectively.

QSG	+/-	*/	T	M
SOGI	4	3	0	2
MSOGI	1+6F	4F	0	2F
MAF	10	13	4	3+2*round(N)
DSC	10	23	6	16*round(N)
2S	2	3	0	2
2S + non-adaptive HF	3+3F	3+4F	0	2+3F
2S + proposed HF	3+7F	3+10F	0	1+4F

*/ = gains, multiplications and divisions, T = trigonometric functions,

M = data memory units and F = number of harmonic orders considered.

Table I: Number of operations and memory units required for the digital implementation.

The performance of the 2S PLLs in case of voltage dips has also been analyzed. Steady-state test conditions have been combined through LHS with different voltage dip depths, in the range *[20% , 90%]*, durations, in the range $[10ms, 200ms]$ and initial phases $[0, 360\text{º})$. The dynamics of the PLLs are evaluated in the falling down transient. The overshoot of the phase error is shown in Fig. 8.a. The performance of the 2S PLL without HF is equivalent to the one observed in the steady-state test (Fig. 4.b). By including the proposed HF stage, the overshoot increases, becoming worst without adaptation capability. Within all the analyzed PLLs with HF capability, best performers are SOGI, DSC and MAF PLLs, with overshoot medians in the range $[0.523\text{º}, 0.563\text{º}]$. The PDFs of the measured response times are shown in Fig. 8.b. The largest median corresponds to the 2S PLL with slow adaptive HF, which can be improved by speeding up the steepest descent algorithm. Overall, the PLLs with SOGI, MSOGI, DSC and MAF perform better than 2S PLLs in presence of voltage dips.

Table 2 summarizes the number of operations and memory units required for the digital implementation of the proposed adaptive filtering stage and the 2S QSG, described in Section II. For comparison purposes, equivalent PLL blocks in other single-phase PLLs with harmonic filtering capability are also evaluated. The 2S QSG, without harmonic filtering structure, requires the fewest operations. By including the harmonic filtering structure, the number of operations and memory units increases depending on F, i.e. the number of voltage harmonics to be filtered out. The DSC and MAF QSGs require a number of data memory units that depends on N and the trigonometric functions. It must be also considered that if the set of harmonic orders is restricted [53], the number of rotation stages of the DSC QSG is reduced accordingly. The difference between the resources in the 2S QSG with non-adaptive and adaptive HF is due to the steepest descent block shown in Fig. 1, included in the adaptive HF and the procedure to adjust the frequency of each observer as a function of N. The SOGI QSG exhibits similar computational burden than the 2S PLL without filtering stage, while the MSOGI performs similarly than the 2S QSG with non-adaptive HF.

IV. EXPERIMENTAL RESULTS

The proposed 2S PLL with harmonic filter is evaluated experimentally using a Full-Bridge AC-DC bidirectional con-
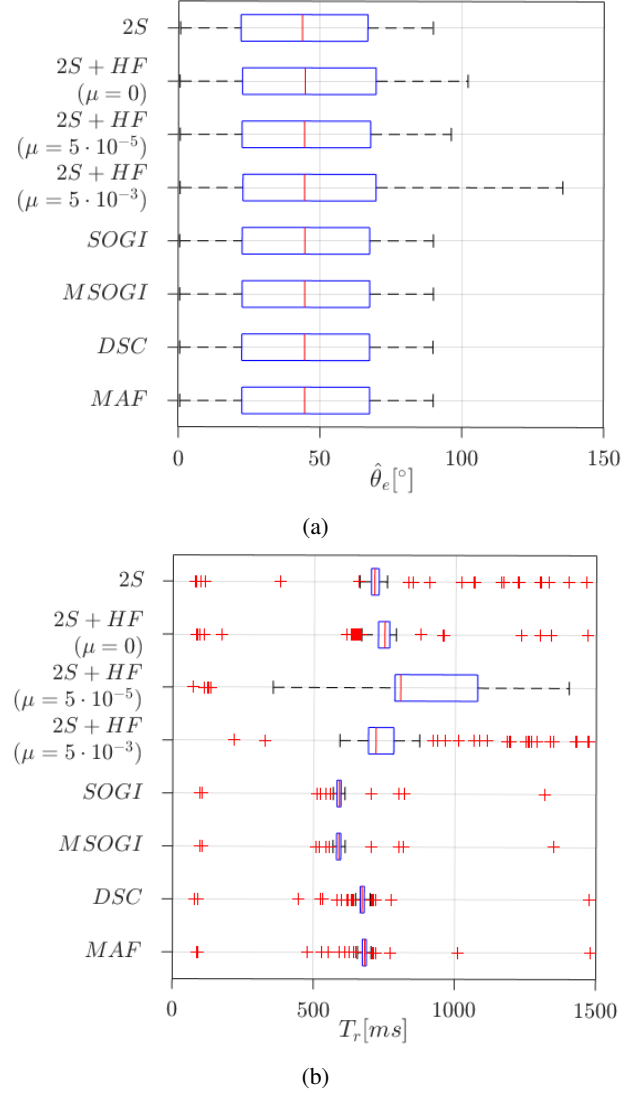

(a)

(b)

Fig. 7: Results of MC tests with phase jumps. Starting phase angle and jump magnitude are varied through LHS.

verter working as an active rectifier. A $500 \ \Omega \ 320W$ DC load is feed through an H-bridge, the output voltage, v_{dc}, and the input current, i_g, are filtered out by means of the output capacitor C ($500 \ uF$) and the input LCL filter ($L_g = 1 \ mH, L_c = 2 \ mH, C_f = 7 \ uF$) respectively. A programmable HP 6841A power source is used to emulate the grid voltages, v_g, for different operation conditions. The digital controller is implemented in a dSpace DS1103, at $f_{sw} = 6.4 \ kHz$, providing the gate signals g_x by means of a unipolar PWM strategy which is used to synchronize the signal acquisition. Hall sensors are used to sense v_g, i_g and v_{dc}. Signal conditioning and antialiasing filtering (4th-order multiple-feedback Butterworth) stages are included.

The digital controller consists of a DC voltage controller, the synchronization subsystem and the current controller. The sensed v_{dc} signal is compared to the reference one ($v_{dc}^* = 400V$) and the error signal is applied to a PI controller ($K_{p_c} = 24e-3$ and $K_{i_c} = 11e3$) which outputs the amplitude of the grid current (I_g^*) required to feed the R_{load} at v_{dc}^*
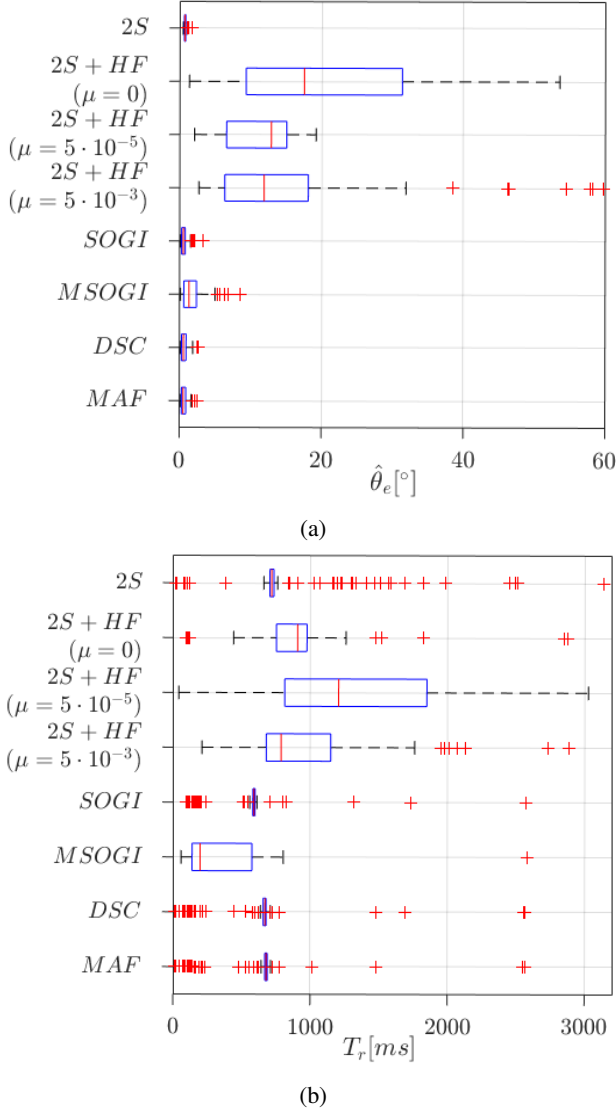
(a)

(b)

Fig. 8: Results of MC tests with voltage dips. Starting phase angle and dip depth and duration are varied through LHS.

. Different synchronization strategies can be tested and, in order to achieve unity power factor, they must provide the signal $\sin(\omega t + \phi_0)$, in-phase with the fundamental of v_g. Then, the reference input current i_g^* is obtained by multiplying I_g^* and $\sin(\omega t + \phi_0)$. The reference current i_g^* is compared to the actual i_g and the error signal is provided to a proportional-resonant controller ($K_{p_c} = 6, K_{i_c} = $ 1e-3) plus a harmonic controller at 3rd, 5th and 7th (with gains $K_3 = K_5 = K_7 = 200$) to compensate for the grid harmonic distortion. The resonance frequency is adjusted dynamically using the value provided by the PLL and all the integral blocks include an anti-windup functionality. The characteristics of each control subsystem have been selected to decouple the effect of other control loops and achieve a good performance during frequency step tests. More details about these controllers can be found in [4]. Three 2S PLLs, with adaptive HF, non-adaptive and without HF, are compared to the SOGI PLL. The configurations of other subsystems within the digital controller are maintained across the tests.

The grid frequency ω exhibits ripple, which moves the resonant peak of the resonant and the harmonic controllers around the actual ω. This effect is mitigated by designing the PLLs to limit the peak-to-peak ripple 20 mHz at 50 Hz. With this objective, the loop filter of the 2S PLL with adaptive HF is tuned following the procedure in [4], [47], resulting in a settling time, T_{set} = 0.6 s. This settling time is also used in the 2S PLL versions with the non-adaptive HF and without filter. The SOGI PLL is tuned according to the procedure in [52] and, then, the selected crossover frequency of the SOGI PLL is set to 1.8 Hz. The results obtained are shown in Fig. 9. The tests conditions are frequency steps from 49 Hz to 51 Hz and harmonically distorted grid voltages (2% , 3% and 2% of the 3rd, 5th and 7th harmonic, respectively). Steady state, before and after the frequency step, and transient responses are evaluated. The best steady state performance (PF = 0.994) is achieved with the SOGI PLL (Fig. 9.d). Close to these values, the 2S PLL with adaptive HF (Fig. 9.a), results in PF = 0.993 and PF = 0.992 at 51 Hz and 49 Hz, respectively. The 2S PLL with non-adaptive HF (Fig. 9.b) reaches the performance of the adaptive version at 51 Hz but, at 49 Hz, the PF becomes the worst ($PF = 0.978$). Due to the tuning procedure followed, all the three PLLs results in equivalent frequency ripples. Maintaining the same settling time in the 2S PLL without harmonic filter results in a higher frequency ripple (Fig. 9.c), which is due to the harmonic distortion passing through the QSG. However, it achieves a relatively high PF at 49 Hz (PF = 0.987).

Transient responses show that, in all the evaluated PLLs, the performance is dominated by the loop filter dynamics. The fastest response is achieved with the 2S PLL without harmonic filter (Fig. 9.c), resulting in a 214 ms transient and a line current peak of 1.1 A over the normal operation conditions. 2S PLLs with harmonic filters result in similar transient responses, with the adaptive version (Fig. 9.a) performing better, 18 ms faster and 0.1 A lower peak current, than the non-adaptive version (Fig. 9.b). In the case of the SOGI PLL, the applied crossover frequency results in the slowest response time (582 ms), the greatest peak current variation (2.5 A) and a frequency peak of +0.8 Hz over the real grid frequency. This behavior can be improved by increasing the crossover frequency, but the frequency ripple would increase accordingly.

V. CONCLUSION

A new harmonic filtering structure has been embedded in the 2S-PLL synchronization circuit, whose original version lacks harmonic filtering capacity. The proposed harmonic filtering is based on observers at each frequency of interest in the grid voltage and each observer is built following the 2S approach. Two versions of this filtering stage have been proposed: non-adaptive and adaptive. The adaptive version adjusts the filter gains dynamically leveraging the steepest descent method, improving the 2S PLL performance in the case of grid voltage events and transients, and increasing the consistency of the 2S PLL performance across different grid conditions. In
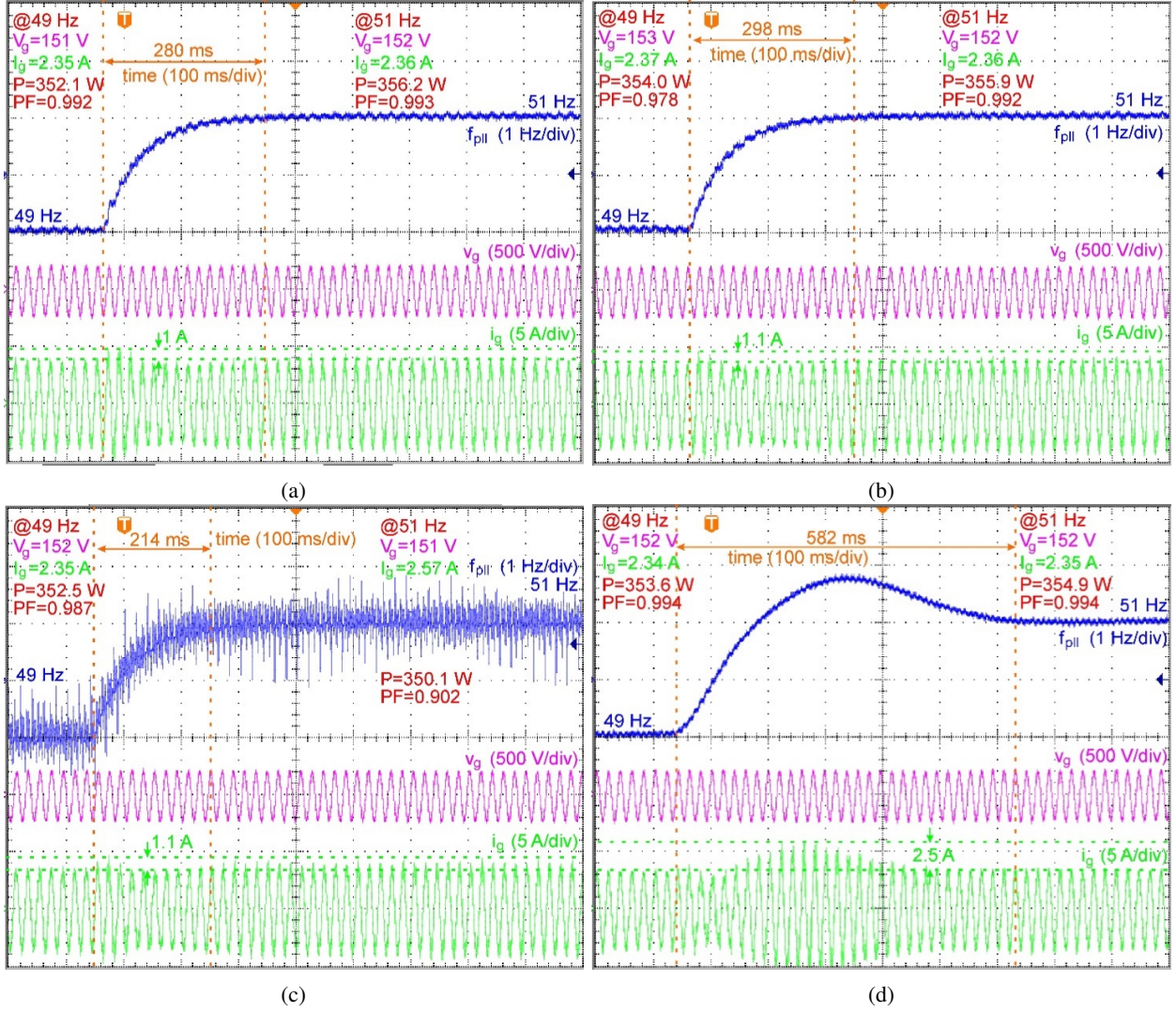
Fig. 9: Line current and voltage waveforms due to a frequency step (2 Hz) and harmonically distorted grid voltage (2% , 3% and 2% of the 3rd, 5th and 7th harmonic, respectively) with a) 2S PLL with adaptive HF, b) 2S PLL with non-adapttive harmonic filtering, c) 2S PLL without harmonic filtering and d) SOGI PLL $f_{crossover} = 1.78$ Hz. PLL frequency: f_{PLL}, dark blue. Grid voltage, v_g, magenta. Line current, i_g, light green.

comparison to other single-phase PLLs with harmonic filtering capability, such as SOGI and MSOGI, the proposal achieves a similar, or superior, performance. The computational burden of the 2S-PLL is higher than other commonly used structures it has been compared to when embedding the harmonic filtering stage, particularly in the adaptive version. However, when the grid harmonic distortion is due to a reduced set of specific harmonics, the proposed approach allows to filter out them while the associated computational burden is kept in the size of other single-phase PLLs counterparts with harmonic filtering capability. By comparing the proposed PLLs with the most similar structures, the MSOGI and 2S PLL with the non-adaptive filtering stage, it performs better in the case of grid frequency ramps and jumps, while the associated computational burdens are similar.

REFERENCES

[1] Y. Lo, T. Lee, and K. Wu, "Grid-Connected Photovoltaic System With Power Factor Correction," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 2224–2227, May 2008.

[2] X. Wang and F. Blaabjerg, "Harmonic Stability in Power Electronic-Based Power Systems: Concept, Modeling, and Analysis," *IEEE Transactions on Smart Grid*, vol. 10, no. 3, pp. 2858–2870, May 2019.

[3] M. H. J. Bollen and I. Y. H. Gu, *Signal Processing of Power Quality Disturbances*. John Wiley & Sons, Aug. 2006, google-Books-ID: cUCDS1DgEgAC.

[4] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*. John Wiley & Sons, Jul. 2011.

[5] B. M. Wilamowski and J. D. Irwin, Eds., *The Industrial Electronics Handbook, Second Edition - Five Volume Set*, 2nd ed. Boca Raton, Fla.; London: CRC Press, Mar. 2011.

[6] F. Vasca and L. Iannelli, Eds., *Dynamics and Control of Switched Electronic Systems*, ser. Advances in Industrial Control. London: Springer London, 2012. [Online]. Available: http://link.springer.com/10.1007/978-1-4471-2885-4

[7] Q.-C. Zhong and T. Hornik, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*, edición: 1 ed. Chichester, West Sussex: John Wiley & Sons, Jan. 2013.

[8] P. Lipnicki, "Smart Grids - General Review of Synchronization Techniques," *IAP GOS,*, vol. 3, pp. 18–23, 2013.

[9] F. D. Freijedo, "Contributions to grid-synchronization techniques for power electronic converters," Ph.D. dissertation, Vigo University, 2009.

[10] N. S. M. L. Marinus, E. C. d. Santos, C. B. Jacobina, N. Rocha, and N. B. d. Freitas, "A Bridgeless Controlled Rectifier for Single Split-Phase Systems," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1–1, 2017.

[11] R. M. B. Cavalcanti, N. Rocha, C. B. Jacobina, N. S. M. L. Marinus, and E. C. d. Santos, "Synchronization method for asymmetrical bridgeless boost rectifier," in *XI Brazilian Power Electronics Conference*, Sep. 2011, pp. 1009–1014.

[12] Y. Liu, Y. Sun, and M. Su, "A Control Method for Bridgeless Cuk/Sepic PFC Rectifier to Achieve Power Decoupling," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[13] Y. Han, M. Luo, X. Zhao, J. M. Guerrero, and L. Xu, "Comparative Performance Evaluation of Orthogonal-Signal-Generators-Based Single-Phase PLL Algorithms—A Survey," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3932–3944, May 2016.

[14] Y. F. Wang and Y. W. Li, "Grid Synchronization PLL Based on Cascaded Delayed Signal Cancellation," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1987–1997, Jul. 2011.

[15] Y. N. Batista, H. E. P. d. Souza, F. A. S. Neves, R. F. D. Filho, and F. Bradaschia, "Variable-Structure Generalized Delayed Signal Cancellation PLL to Improve Convergence Time," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7146–7150, Nov. 2015.

[16] Y. Lu, G. Xiao, X. Wang, and F. Blaabjerg, "Grid Synchronization With Selective Harmonic Detection Based on Generalized Delayed Signal Superposition," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3938–3949, May 2018.

[17] S. Golestan, M. Ramezani, J. M. Guerrero, and M. Monfared, "dq-Frame Cascaded Delayed Signal Cancellation- Based PLL: Analysis, Design, and Comparison With Moving Average Filter-Based PLL," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1618–1632, Mar. 2015.

[18] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, and J. Doval-Gandoy, "An Efficient Implementation of Generalized Delayed Signal Cancellation PLL," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1085–1094, Feb. 2016.

[19] Y. F. Wang and Y. Wei Li, "Analysis and Digital Implementation of Cascaded Delayed-Signal-Cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067–1080, Apr. 2011. [Online]. Available: http://ieeexplore.ieee.org/document/5624643/

[20] H. A. Hamed, A. F. Abdou, E. H. E. Bayoumi, and E. E. EL-Kholy, "Frequency Adaptive CDSC-PLL Using Axis Drift Control Under Adverse Grid Condition," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2671–2682, Apr. 2017.

[21] J. Wang, J. Liang, F. Gao, L. Zhang, and Z. Wang, "A Method to Improve the Dynamic Performance of Moving Average Filter-Based PLL," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5978–5990, Oct. 2015.

[22] S. Golestan, J. M. Guerrero, A. M. Abusorrah, and Y. Al-Turki, "Hybrid Synchronous/Stationary Reference-Frame-Filtering-Based PLL," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 5018–5022, Aug. 2015.

[23] Q. Huang and K. Rajashekara, "An Improved Delayed Signal Cancellation PLL for Fast Grid Synchronization Under Distorted and Unbalanced Grid Condition," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4985–4997, Sep. 2017.

[24] N. Hui, D. Wang, and Y. Li, "A Novel Hybrid Filter-Based PLL to Eliminate Effect of Input Harmonics and DC Offset," *IEEE Access*, vol. 6, pp. 19 762–19 773, 2018. [Online]. Available: http://ieeexplore.ieee.org/document/8329237/

[25] Y. Li, D. Wang, W. Han, S. Tan, and X. Guo, "Performance Improvement of Quasi-Type-1 PLL by using a Complex Notch Filter," *IEEE Access*, vol. 4, pp. 6272–6282, 2016.

[26] C. Zhang, X. Zhao, X. Wang, X. Chai, Z. Zhang, and X. Guo, "A Grid Synchronization PLL Method Based on Mixed Second- and Third-Order Generalized Integrator for DC Offset Elimination and Frequency Adaptability," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1517–1526, Sep. 2018.

[27] F. Xiao, L. Dong, L. Li, and X. Liao, "A Frequency-Fixed SOGI-Based PLL for Single-Phase Grid-Connected Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017.

[28] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, A. Bakhshai, and M. Mojiri, "Addressing DC Component in PLL and Notch Filter Algorithms," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 78–86, Jan. 2012.

[29] J. R. d. Carvalho, C. A. Duque, M. V. Ribeiro, A. S. Cerqueira, T. L. Baldwin, and P. F. Ribeiro, "A PLL-Based Multirate Structure for Time-Varying Power Systems Harmonic/Interharmonic Estimation," *IEEE Transactions on Power Delivery*, vol. 24, no. 4, pp. 1789–1800, Oct. 2009.

[30] K. Lee, J. Lee, D. Shin, D. Yoo, and H. Kim, "A Novel Grid Synchronization PLL Method Based on Adaptive Low-Pass Notch Filter for Grid-Connected PCS," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 292–301, Jan. 2014.

[31] P. Kanjiya, V. Khadkikar, and M. S. E. Moursi, "A Novel Type-1 Frequency-Locked Loop for Fast Detection of Frequency and Phase With Improved Stability Margins," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2550–2561, Mar. 2016.

[32] B. Liu, F. Zhuo, Y. Zhu, H. Yi, and F. Wang, "A Three-Phase PLL Algorithm Based on Signal Reforming Under Distorted Grid Conditions," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5272–5283, Sep. 2015.

[33] J.-P. Lee, B.-D. Min, T.-J. Kim, D.-W. Yoo, and J.-Y. Yoo, "Active Frequency with a Positive Feedback Anti-Islanding Method Based on a Robust PLL Algorithm for Grid-Connected PV PCS," *Journal of Power Electronics*, vol. 11, no. 3, May 2011.

[34] C. Subramanian and R. Kanagaraj, "Rapid Tracking of Grid Variables Using Prefiltered Synchronous Reference Frame PLL," *IEEE Transactions on Instrumentation and Measurement*, vol. 64, no. 7, pp. 1826–1836, Jul. 2015.

[35] B. P. McGrath, D. G. Holmes, and J. J. H. Galloway, "Power converter line synchronization using a discrete Fourier transform (DFT) based on a variable sample rate," *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 877–884, Jul. 2005.

[36] P. Sumathi and P. A. Janakiraman, "Integrated Phase-Locking Scheme for SDFT-Based Harmonic Analysis of Periodic Signals," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 1, pp. 51–55, Jan. 2008.

[37] I. Carugati, S. Maestri, P. G. Donato, D. Carrica, and M. Benedetti, "Variable Sampling Period Filter PLL for Distorted Three-Phase Systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 321–330, Jan. 2012.

[38] I. Carugati, P. Donato, S. Maestri, D. Carrica, and M. Benedetti, "Frequency Adaptive PLL for Polluted Single-Phase Grids," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2396–2404, May 2012.

[39] G. D. Donato, G. Scelba, G. Borocci, F. G. Capponi, and G. Scarcella, "Fault-Decoupled Instantaneous Frequency and Phase Angle Estimation for Three-Phase Grid-Connected Inverters," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2880–2889, Apr. 2016.

[40] M. Karimi-Ghartemani and M. R. Iravani, "Measurement of harmonics/inter-harmonics of time-varying frequencies," *IEEE Transactions on Power Delivery*, vol. 20, no. 1, pp. 23–31, Jan. 2005.

[41] M. Mojiri, M. Karimi-Ghartemani, and A. Bakhshai, "Processing of Harmonics and Interharmonics Using an Adaptive Notch Filter," *IEEE Transactions on Power Delivery*, vol. 25, no. 2, pp. 534–542, Apr. 2010.

[42] D. Shin, K. Lee, J. Lee, D. Yoo, and H. Kim, "Implementation of Fault Ride-Through Techniques of Grid-Connected Inverter for Distributed Energy Resources With Adaptive Low-Pass Notch PLL," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2859–2871, May 2015.

[43] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A Robust Synchronization to Enhance the Power Quality of Renewable Energy Systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4858–4868, Aug. 2015.

[44] K. Selvajyothi and P. A. Janakiraman, "Extraction of Harmonics Using Composite Observers," *IEEE Transactions on Power Delivery*, vol. 23, no. 1, pp. 31–40, Jan. 2008.

[45] N. R. N. Ama, F. O. Martinz, L. Matakas, and F. Kassab, "Phase-Locked Loop Based on Selective Harmonics Elimination for Utility Applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 144–153, 2013.

[46] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An Adaptive Synchronous-Reference-Frame Phase-Locked Loop for Power Quality Improvement in a Polluted Utility Grid," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 6, pp. 2718–2731, Jun. 2012.

[47] P. Lamo, F. López, A. Pigazo, and F. J. Azcondo, "An Efficient FPGA Implementation of a Quadrature Signal-Generation Subsystem in SRF PLLs in Single-Phase PFCs," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3959–3969, May 2017.

[48] P. Lamo, A. Pigazo, G. A. Ruiz, F. J. Azcondo, and F. López, "An Optimized Implementation of a Two-Sample Phase Locked Loop with Frequency Feedback for Single-Phase Sensorless Bridgeless PFC," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2018, pp. 1–6.

[49] B. Widrow, *Adaptive Signal Processing*, edición: 1st ed. Noida: Pearson, Mar. 1985.

[50] S. Haykin and B. Widrow, *Least-Mean-Square Adaptive Filters*, edición: 1 ed. Hoboken, N.J: Wiley-Interscience, Sep. 2003.

[51] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics Assessment of Advanced Single-Phase PLL Structures," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013.

[52] P. Rodríguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 127–138, Jan. 2011, conference Name: IEEE Transactions on Industrial Electronics.

[53] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "Advanced Single-Phase DSC-Based PLLs," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3226–3238, Apr. 2019, conference Name: IEEE Transactions on Power Electronics.

[54] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "A Nonadaptive Window-Based PLL for Single-Phase Applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 24–31, Jan. 2018.

[55] U.-E. 50160, "Voltage characteristics of electricity supplied by public distribution systems," 1999.

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