Thermal balancing of multiphase battery chargers controlled by phase shift

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HIGHLIGHTS

- Multiphase architecture with reduced conduction losses.
- Phase-shift control at constant switching frequency.
- The thermal balancing control equalizes the temperature of all components.
- The converter exhibits a nearly constant efficiency across a wide load range.

GRAPHICAL ABSTRACT
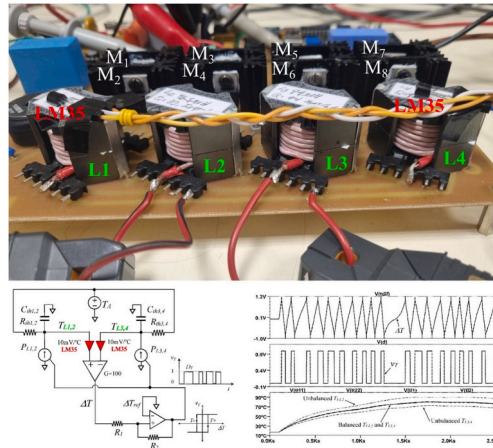
ARTICLE INFO

ABSTRACT

Power sources based on multiphase resonant converters, controlled by phase-shift at constant switching frequency, reduce conduction losses and enable current-mode operation for battery charger applications. However, phase-shift modulation in multiphase class D resonant converters inherently causes uneven current distribution among sections, leading to a thermal imbalances in transistors and inductors. To address this, a thermal balancing control strategy is proposed, which equalizes temperatures by modulating the amplitude (AM) of the resonant currents flowing through the transistors and inductors in each Class D section. A simple hysteresis band outer controller set up the average phase shift required to balance the temperature in the resonant branches. This method involves periodically exchanging the control signals of the inverter sections, which does not affect the output variables due to the symmetrical structure of the circuit. Thus, this approach enables thermal management without interfering with the inner output variable control set by the instantaneous phase shift. The proposal

is validated experimentally using a four-phase LC_pC_s resonant converter designed for a Lithium-ion battery charger application.

1. Introduction

Lithium iron phosphate (LiFePO$_4$) batteries exhibit excellent thermal stability and electrochemical performance, rendering this technology both safe and robust [1]. LiFePO$_4$ batteries are mainly used in storage systems for renewable energy facilities, electric vehicles, and uninterruptible power supplies (UPS) [2,3]. The current capacity (C_n) of the LiFePO$_4$ technology reaches rates as high as hundreds of amps [4]. The battery charger should meet all specifications required for circuits at high-current applications, where conduction losses are a significant design issue [5]. The multiphase resonant converter architecture [6] and interleaved structures [7] have been widely adopted in industrial applications due to their high current capacity. Besides battery chargers, examples include induction heating, wireless energy transmission, and welding machines [8,9]. The multiphase inverter architecture distributes the output current among the different phases, minimizing conduction losses.

Additionally, this architecture enables precise control of the output parameter at a constant switching frequency through the phase-shift control of output voltages from each class D section of the inverter. The concept of phase-shift control, also known as outphasing modulation, was initially proposed in the early 1930s by Chireix to enhance the efficiency and linearity of AM radio transmitters [10]. In outphasing architecture, transmitters generate a variable output by manipulating the phases of the input signals sent to linear power amplifiers. The same principle is extended to multiphase DC-DC resonant power converters [11].

Despite the advantages of constant switching frequency operation, particularly in terms of magnetic component design and switching loss optimization, phase-shift control inherently results in uneven current distribution due to the varying amplitude of the resonant currents. This imbalance can eventually cause thermal issues in the transistors and inductors of the Class D sections [12]. Operating under thermally unbalanced conditions increases the risk of converter failure, as repeated exposure to high temperatures accelerates the ageing of inductors and transistors, thereby reducing the components' mean time between failures (MTBF) [13–15]. Similar thermal imbalance issues also arise in other DC-DC converter topologies, such as multilevel and interleaved designs [16,17].

This work proposes a thermal balancing strategy [18] based on the AM modulation of the resonant currents within each class D section of the inverter. This outer thermal balancing control (TBC) is fully compatible with the inner control of the converter's electrical variables.

The contributions of this work are highlighted in the following points:

- The multiphase architecture of a power source based on a resonant inverter stage with reduced conduction losses and high output current capability.
- The multiphase architecture enables the phase-shift control of the output current at constant switching frequency.
- The thermal imbalance is eliminated by an external thermal balancing control loop that equalizes the temperature across all components in the resonant inverter stage. The proposed hysteresis band control enables the exchange of command signals between inverter sections with a quasi-seamless transition, resulting in negligible variation in the output current.

The paper is organized as follows: after the introduction, Section 2 analyzes a multiphase resonant converter proposed as a battery charger, focusing on the current distribution among the different class D sections.

The proposal to address thermal imbalance is presented in Section 3. The design of the inverter and rectifier stages is explained in Sections 4 and 5. Experimental results are presented in Section 6, finalizing with the conclusions.

2. Multiphase LC_pC_s resonant converter

The benefits of resonant converters, particularly in terms of high-frequency operation and low switching losses, are well established [11]. Among all possible configurations of resonant converters, the *CLLC* and the *LLC* topologies have been widely used for battery charger applications [19–22]. In both configurations, the converter is designed to operate as a voltage source with a controller limiting the charging current. In this work, a four-phase parallel-series LC_pC_s resonant converter is proposed as a voltage-dependent current source, featuring an inherent current limitation that ensures a safer operation. On the other hand, the multiphase structure is scalable to higher power levels by adding additional phases [6]. For the power level considered in this battery charger application, a four-phase configuration offers a moderately cost-effective solution, particularly well-suited to silicon transistors. Fig. 1 (a) illustrates a four-phase LC_pC_s resonant converter with a current-doubler rectifier at the output stage for further efficiency improvement. The battery is modeled using an electrical parameters-based approach [23]. In steady-state conditions and for a given state of charge (*SoC*) [24], the equivalent circuit model is simplified to the internal impedance of the battery, r_{Bat} [25], and the quasi-open-circuit voltage, $V_{qoc}(SoC)$ [26].

The circuit is analyzed using the fundamental harmonic approximation (FHA). Fig. 1 (b) shows a simplified representation of the circuit. The midpoint square voltages (at nodes 1 to 4 in Fig. 1 (a)) are replaced by their first-harmonic components, denoted as v_1 to v_4. The current-doubler rectifier is modeled by its equivalent impedance, R_{ac}, as reflected on the primary side of the transformer. The parasitic equivalent resistance, r, includes the equivalent series resistance (ESR) of inductors, r_L, the $R_{ds(on)}$ of transistors, the resistance of the printed circuit board (PCB), r_B, and other parasitic elements.

### 2.1. Study of the distribution of currents at the resonant inverter stage

In this research, the output current of the converter is controlled by adjusting the phase shift of the midpoint voltages $v_{1,2,3,4}$ by pairs ($v_1 = v_2$ and $v_3 = v_4$), dividing the resonant inverter stage into two symmetric halves, i.e., $\Psi_0 = \Psi_1$ and $\Psi_2 = \Psi_3$. This approach requires only two drive signals, with the control angle, Ψ, defined as the phase shift between $v_{1,2}$ and $v_{3,4}$, i.e., $\Psi = \Psi_2 - \Psi_0 = \Psi_3 - \Psi_1$. Voltage phasors V_1 to V_4 for FHA are then given by

$$V_{1,2} = \frac{2V_{dc}}{\pi}e^{+j\frac{\Psi}{2}}, \quad V_{3,4} = \frac{2V_{dc}}{\pi}e^{-j\frac{\Psi}{2}}. \tag{1}$$

The resonant inverter stage is fully characterized by the parallel parameters listed in Table 1.

The LC_pC_s resonant inverter exhibits a current source behavior operating at the resonance frequency, ω_p, while maintaining zero-voltage switching (ZVS) over a wide range of loads. The phasor of the output current on the primary side, I_{ac}, is obtained in (2) as a function of the DC-link voltage, V_{dc}, the characteristic impedance of the resonant tank, Z_p, and the control angle, Ψ. Consistent with the current source behavior of the converter at ω_p, (2) exhibits no dependence on Q_p.

$$I_{ac} = -j\frac{8V_{dc}}{\pi Z_p}\cos\frac{\Psi}{2} \tag{2}$$

(a)

(b)
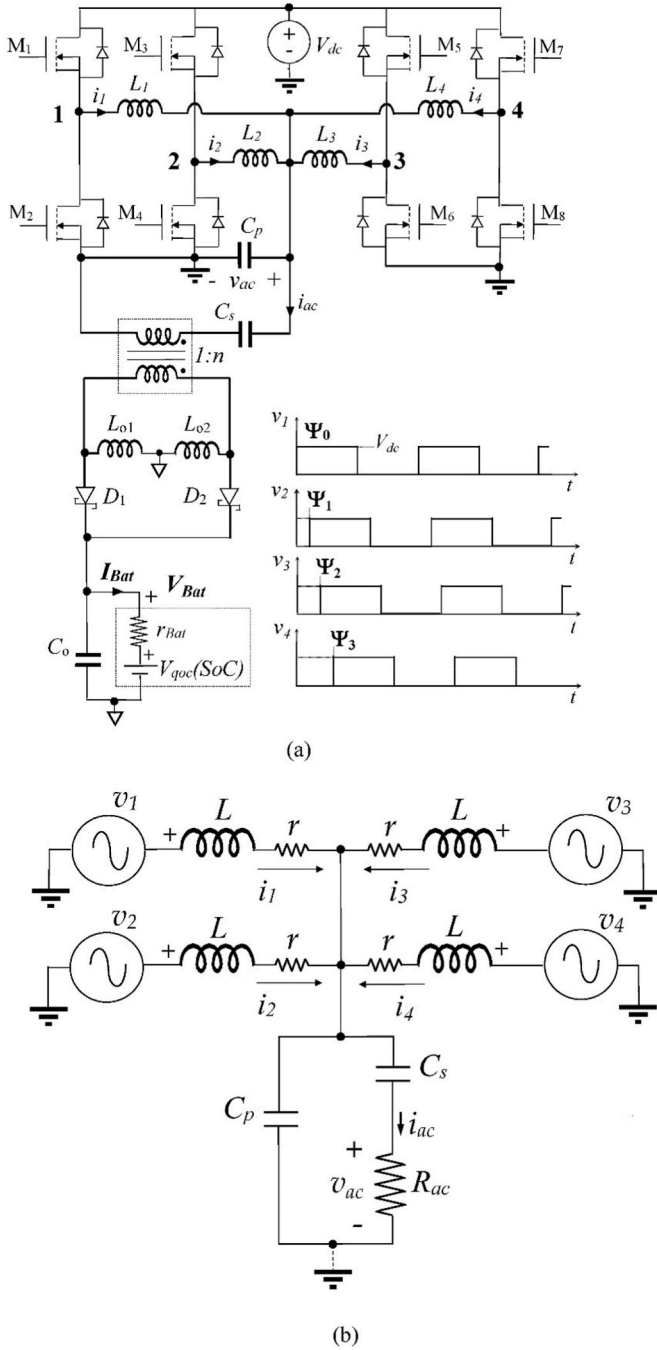
Fig. 1. (a) A four-phase LC_pC_s resonant converter proposed as a battery charger with midpoint voltages, v_1 to v_4, for each class D section. (b) Simplified circuit model applying the FHA for studying the current distribution in the resonant inverter stage.

Table 1
Parallel parameters of the LC_pC_s resonant converter.

Resonant frequency	Characteristic impedance	Quality factor
$\omega_p = \dfrac{1}{\sqrt{\frac{LC_p}{4}}}$	$Z_p = \omega_p L = \dfrac{4}{\omega_p C_p}$	$Q_p = \dfrac{4R_{ac}}{Z_p}$

Using this approach, the circuit inherently limits the maximum current to $\hat{I}_{ac} = 8V_{dc}/\pi Z_p$ when $\Psi = 0°$, resulting in a safe operation mode for battery chargers. The current limit is defined based on the

manufacturer's recommendations provided in the battery user manual. From (2), the regulation of the charging current is carried out at a constant switching frequency, ω_p, by adjusting Ψ. The phasors of the input currents through inductors L_1 to L_4, as a function of the DC-link voltage, V_{dc}, the characteristic impedance of the resonant tank, Z_p, the quality factor, Q_p, and the control angle, Ψ, are given by

$$I_{1,2} = \frac{2V_{dc}}{\pi Z_p}\left[Q_p\cos\frac{\Psi}{2} + \sin\frac{\Psi}{2} - j\left(1 + \frac{C_p}{C_s}\right)\cos\frac{\Psi}{2}\right] \quad (3)$$

and

$$I_{3,4} = \frac{2V_{dc}}{\pi Z_p}\left[Q_p\cos\frac{\Psi}{2} - \sin\frac{\Psi}{2} - j\left(1 + \frac{C_p}{C_s}\right)\cos\frac{\Psi}{2}\right]. \quad (4)$$

During the constant current (CC) stage of the charging profile [27], if the circuit supplies the maximum charging current (full power operation), $\Psi = 0°$ and, from (3) and (4), the phase currents are balanced, $\hat{I}_{1,2} = \hat{I}_{3,4}$. The amplitude of the output current, $\hat{I}_{ac}$, is approximately four times the amplitude of each of the resonant currents $\hat{I}_{1,2}$ and $\hat{I}_{3,4}$. This feature is highly advantageous since the balanced distribution of the current among the resonant sections minimizes the conduction losses, P_r, associated with the parasitic equivalent resistance, r. The efficiency of the multiphase resonant inverter stage, considering only the conduction losses, is given by (5), where P_{ac} is the power delivered to the equivalent load, R_{ac}.

$$\eta_I = \frac{1}{1 + \frac{P_r}{P_{ac}}} \quad (5)$$

In contrast, at any other charging current level or during the constant voltage (CV) stage, the charging current must be regulated via Ψ to maintain the battery voltage at $V_{B(Max)}$. From (3) and (4), varying Ψ results in a current imbalance between the resonant currents at each converter half, i.e., $\hat{I}_{1,2} \neq \hat{I}_{3,4}$. The amplitude of phasors given in (2), (3) and (4), normalized by $2V_{dc}/\pi Z_p$, are plotted in Fig. 2 (a). The normalized magnitude of the resonant current imbalance between branches 1,2 and 3,4, $\hat{I}_{1,2}$-$\hat{I}_{3,4}$, as a function of Ψ and Q_p is illustrated in Fig. 2(b).

As Ψ increases, a significant difference between the amplitude of the resonant currents $i_{1,2}$ and $i_{3,4}$ is observed. The angle Ψ_Δ, at which the current imbalance is maximized, is obtained in (6).

$$\Psi_\Delta = 2\,arccos\left(\sqrt{\frac{2}{4 + Q_p^2}}\right) \quad (6)$$

For $Q_p < 1$, the current imbalance reaches its peak around $\Psi = \Psi_\Delta = 90°$. The current imbalance is the primary mechanism responsible for uneven heating of components within each Class D section. Class D sections operating at higher temperatures than others may require larger inductors and heat sinks, leading to increased costs and negatively impacting overall circuit reliability. Solutions aimed at achieving equal current sharing in multiphase resonant converters, such as the use of balancing or intercell transformers, have been reported in Refs. [8,28]. However, these approaches require custom magnetic cores, which increase cost and complexity while reducing power density. Moreover, current balancing alone does not ensure uniform temperature distribution due to asymmetries in the thermal path, component and assembly tolerances, and PCB layout.

3. Thermal balancing control

In this work, the proposal to achieve the thermal balance leverages the symmetric structure of the converter. By considering the parity of the trigonometric functions in (3) and (4), it can be observed from Fig. 2 (a) that $\hat{I}_{1,2} > \hat{I}_{3,4}$ for Ψ and $\hat{I}_{1,2} < \hat{I}_{3,4}$ for $-\Psi$, respectively. However, due to the symmetric structure of the inverter stage, the absolute value of the control angle determines the amplitude of the output current, $\hat{I}_{ac}$. This

(a)

(b)
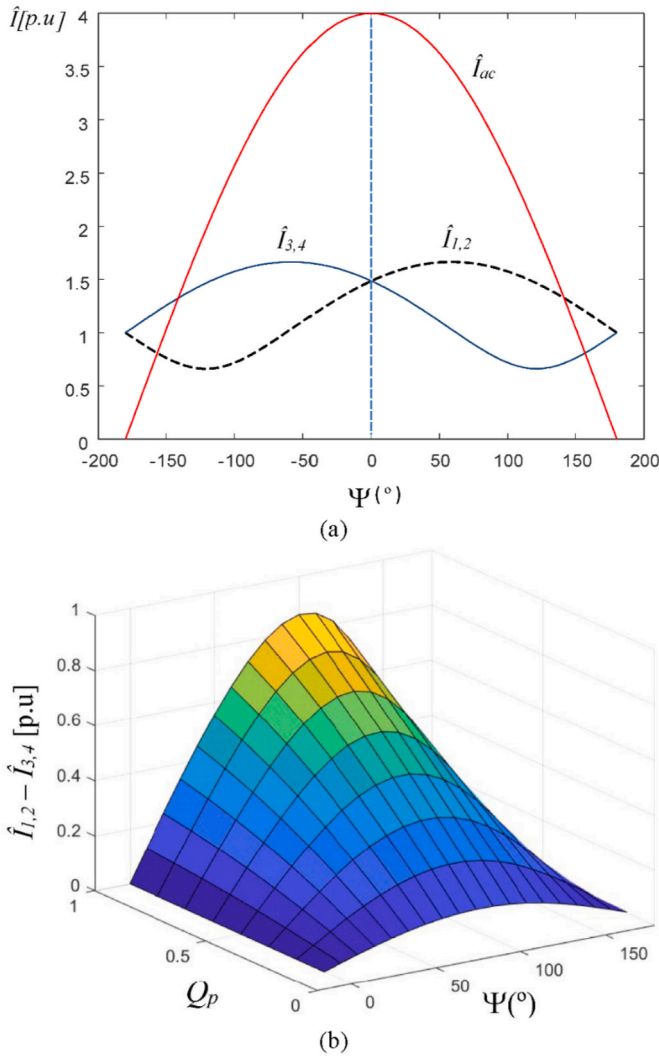
Fig. 2. (a) The normalized amplitude of resonant currents $\hat{I}_{1,2}$ and $\hat{I}_{3,4}$ and the output current in the primary side $\hat{I}_{ac}$ as a function of Ψ. The capacitor ratio is $C_p/C_s = 0.1$ and $Q_p = 0.5$. (b) Difference, normalized with $2V_{dc}/\pi Z_p$, between the resonant currents of branches 1,2 and 3,4 as a function of Ψ and Q_p.

property enables amplitude modulation (AM) of the resonant currents, thereby balancing the average current stress across the resonant branches. This is achieved by periodically exchanging the drive signals [29] between each half of the converter without affecting the output current. The exchange of control signals is governed by a thermal management signal, v_T, which operates with a duty cycle, D_T, and frequency, $f_T = 1/T_T$, as illustrated in Fig. 3(a). The thermal duty cycle, $D_T \in [0,1]$, defines the relative duration of the phase shift Ψ over $-\Psi$, establishing the required average phase shift Ψ_{av}, to compensate for temperature differences between the two sides. Considering that T_T is the integration time window and that the unsigned control angle, Ψ, for adjusting $\hat{I}_{ac}$ remains unchanged during T_T, i.e., $\Psi(t) = \Psi$, the average phase shift, Ψ_{av}, is given by (7).

$$\Psi_{av} = \Psi \cdot D_T - \Psi(1 - D_T) \tag{7}$$

Given the high thermal inertia, on the order of seconds, the frequency of the thermal management signal, v_T, is significantly lower than the converter's switching frequency, i.e., $f_T < \omega_p/2\pi$. The AM of the resonant currents modifies their rms values according to (8) and (9), modulating the losses on both sides of the converter, which eliminates the temperature imbalances in inductors and transistors caused by phase shift modulation.

$$I_{1,2(rms)} = \sqrt{\frac{\hat{I}_{3,4}^2}{2}D_T + \frac{\hat{I}_{1,2}^2}{2}(1 - D_T)} \tag{8}$$

$$I_{3,4(rms)} = \sqrt{\frac{\hat{I}_{1,2}^2}{2}D_T + \frac{\hat{I}_{3,4}^2}{2}(1 - D_T)} \tag{9}$$

If the dispersion in the parasitic resistance value, r, is low, a duty cycle $D_T = 0.5$ is sufficient to achieve thermal balance across all class D sections of the inverter stage. Notably, in practical applications, Ψ_{av} will typically be zero or close to zero, corresponding to D_T equal to or close to 0.5. Although most thermal imbalances can be corrected by equalizing the currents, asymmetries in the parasitic resistances or the thermal circuit may prevent the complete cancellation of the thermal imbalance. To more effectively minimize thermal imbalance, the duty cycle, D_T, of the thermal management signal, v_T, should be adjusted by a control loop. The proposed solution directly addresses thermal imbalance by employing a hysteresis band control strategy [30]. This method was chosen for its inherent stability, simplicity, and suitability for the slow dynamics of thermal transients. In the resonant inverter stage, the inductors are the components that reach the highest temperatures, so they will be used to obtain the thermal model of the circuit. The total power loss in the inductor, P_L, is composed of the winding loss, P_W, and the core loss, P_C; thus, $P_L = P_C + P_W$. By adjusting D_T, the inductor losses on both

(a)

(b)
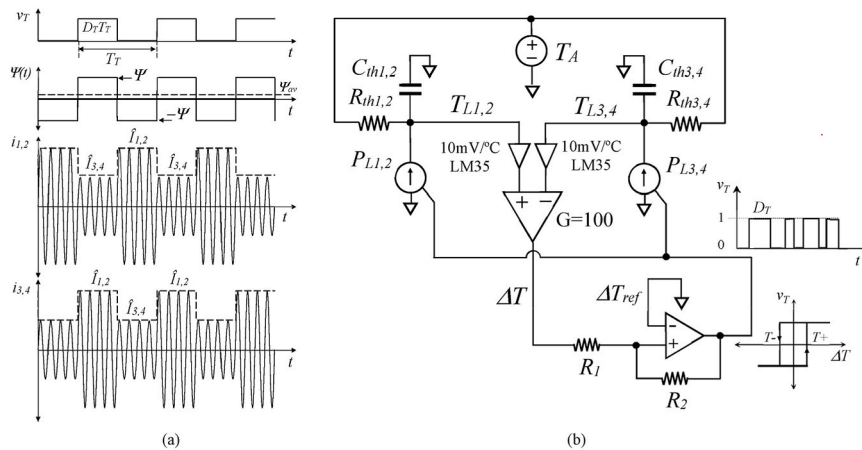
Fig. 3. (a). AM of the resonant currents in branches 1,2, and 3,4 of the inverter stage. (b). Scheme of the control loop by hysteresis band to minimize the temperature imbalance regardless of circuit asymmetries.

sides of the converter are modulated according to (10) and (11), achieving proper thermal balance between the inverter halves. The inductor core loss, P_C, is less dependent on the current and is therefore assumed to remain constant.

$$P_{L1,2} = r_{L1,2}\left[\frac{\widehat{I}_{3,4}^2}{2}D_T + \frac{\widehat{I}_{1,2}^2}{2}(1-D_T)\right] + P_C \qquad (10)$$

$$P_{L3,4} = r_{L3,4}\left[\frac{\widehat{I}_{1,2}^2}{2}D_T + \frac{\widehat{I}_{3,4}^2}{2}(1-D_T)\right] + P_C \qquad (11)$$

The proposed thermal balancing control, based on a hysteresis band strategy, is illustrated in Fig. 3(b), where T_A represents the ambient temperature.

A simplified first-order thermal model for the inductors is proposed to characterize temperature variations. If the core and winding temperatures match, i.e., $T_W = T_C = T_L$, any heat transfer through the core to winding thermal resistance, R_{th_CW}, is neglected. Then, the equivalent thermal impedance is obtained from $1/R_{th} = 1/R_{th\_CA} + 1/R_{th\_WA}$. The equivalent thermal capacitance is $C_{th} = C_{th\_C} + C_{th\_W}$. In Fig. 3(b), the temperatures of inductors L_1 and L_4 in branches 1 and 4 are measured using the integrated circuit LM35. Observing the circuit symmetry, they are assumed to be equal to the temperature of the corresponding inverter halves, $T_{L1,2}$ and $T_{L3,4}$. The acquisition of the temperature difference using a differential amplifier completes the control scheme, $\Delta T = T_{L1,2} - T_{L3,4}$, whose value is constrained between maximum and minimum limits, centered around $\Delta T_{ref} = 0$. Even when using a narrow hysteresis band, ΔT_H, to minimize temperature imbalance, ΔT, the switching of control signals governed by v_T occurs at a low frequency and does not interfere with the converter's operation. The thermal management signal, v_T, is directly obtained from the output of the hysteresis comparator.

4. Design of the resonant inverter stage

The design fulfils all the requirements for charging a commercial 48NPFC100C LiFePO$_4$ battery module, which is selected as a benchmark due to its suitability for a wide range of battery charging requirements. The charging profile follows the recommended two-stage approach: constant current and constant voltage (CC-CV) [27]. According to the user manual [31], the battery module consists of 15 cells connected in series and includes a Battery Management System (BMS) that ensures proper charge balancing among the cells, as well as protection against overcharging and deep discharge. The experimental 10 A charging profile, for the 48NPFC100C battery module is shown in Fig. 4. The battery has a capacity of $C_n = 100$ Ah and a nominal voltage of 48 V. The charging current is set to $C_n/10 = 10$ A (Fig. 4(a)), and the battery voltage is limited to $V_{B(Max)} = 52$ V (Fig. 4 (b)). The maximum power delivered to the battery is 520 W (Fig. 4(c)). The temperature increase of the battery module during charging was measured using two type-T thermocouples: one placed at the center of the external casing and the other used as a reference to measure the room temperature.

The selected charging profile minimizes the increase in battery module temperature during the charging process (Fig. 4(d)), thereby preventing battery degradation and reducing the risk of thermal runaway [27,32].

Switching losses are minimized by ensuring the transistors operate in ZVS mode on the converter's primary side [33]. The ZVS mode requires sufficient phase delay of the resonant currents, $i_{1,2}$ and $i_{3,4}$, relative to the input voltages, $v_{1,2}$ and $v_{3,4}$, respectively. The minimum value of power factor angle for achieving ZVS, φ_{zvs}, is given in (12) and depends on the dead time, t_d, of the transistors' driver and ω_p:

$$\varphi_{zvs} = \frac{t_d\omega_p}{2\pi}\cdot360^0 \qquad (12)$$

Under nominal conditions, a power factor angle value, $\phi_n = 2\varphi_{zvs}$, is assumed as a design criterion. This conservative criterion defines the
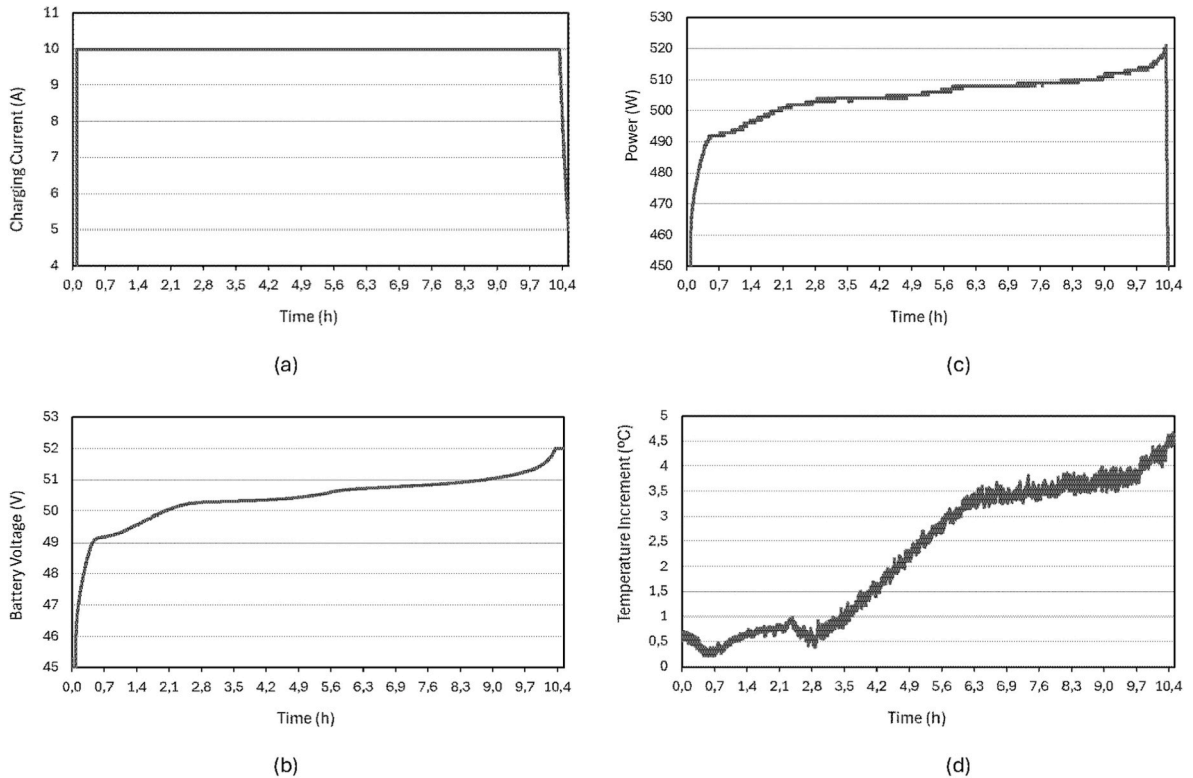
Fig. 4. (a). Charging current profile. The maximum current is set at $C_n/10 = 10$ A. (b) Variation of the battery voltage during the charging process. (c) Power is delivered to the battery during the charging process. (d) The temperature increment of the battery during the charging process.

quality factor, Q_p, and the efficiency, ensuring a reliable converter operation despite heavy load variations during the battery charging process.

$$Q_p = \frac{1}{\tan 2\varphi_{zvs}} \tag{13}$$

The transformer's turn ratio, n, to meet this condition is calculated according to (14):

$$n = \frac{\pi^2 V_{Bat(Max)} \tan 2\varphi_{zvs}}{2V_{dc}} \tag{14}$$

The multiphase solution for the resonant inverter stage achieves an efficiency of more than 90 % using low-cost transistors, even at relatively low values of V_{dc} and n close to unity. The maximum efficiency of the resonant inverter stage is obtained at $\Psi = 0^o$ at the boundary between CC and CV charging stages, where the output power P_{Bat} is the maximum, $P_{Bat(Max)} = 535$ W. Efficiency, as given in (15), is obtained as a function of the design parameters by developing (5), where P_{Bat} is the power delivered to the battery, and N is the number of phases, i.e. $N = 4$,

$$\eta_I = \frac{1}{1 + \frac{\pi^2 r P_{Bat}}{2N V_{dc}^2}\left(1 + \tan^2 2\varphi_{zvs}\right)}. \tag{15}$$

5. Design of the current doubler rectifier

The current-doubler rectifier, which serves as the output stage of the circuit shown in Fig. 1(a), was selected to enhance performance in high-current applications by minimizing the transformer current [34]. The low output voltage of this application allows for the use of Schottky diodes, thereby eliminating the need for a control circuit on the secondary side. The amplitude of the current ripple in inductors L_{o1} and L_{o2} is determined by

$$\Delta i_L = \frac{(\pi - 1)V_{Bat(Max)}}{\omega_p L_o}. \tag{16}$$

From (16) and considering the ripple voltage in the filter capacitor C_o, the ripple of the charging current is obtained in (17) as a function of the switching frequency, the output filter components and battery parameters

$$\Delta i_{Bat} = \frac{\pi(\pi - 1)V_{Bat(Max)}}{16 r_{Bat} \omega_p^2 L_o C_o}. \tag{17}$$

Since the output filter suppresses the high-frequency ripple, Δi_{Bat}, the low ripple approximation is applied to study the rectifier in steady-state. Using the approximation of the first harmonic, the amplitude of the primary side current, i_{ac}, as a function of the DC output current, I_{Bat}, is given by,

$$\widehat{I}_{ac} = \frac{2nI_{Bat}}{\pi}. \tag{18}$$

The amplitude of the voltage at the primary side of the transformer is obtained from the transformer power balance and expressed as a function of the battery parameters,

$$\widehat{V}_{ac} = \frac{\pi}{n}V_{Bat} = \frac{\pi^2}{2n^2}r_{Bat}\widehat{I}_{ac} + \frac{\pi}{n}V_{qoc}. \tag{19}$$

From (18) and (19), the current-doubler rectifier represents an equivalent load, R_{ac}, reflected on the primary side of the transformer,

$$R_{ac} = \frac{\pi^2}{2n^2}R_{Bat} = \frac{\pi^2}{2n^2}\left(r_{Bat} + \frac{V_{qoc}}{I_{Bat}}\right). \tag{20}$$

Conduction losses are predominant in the output rectifier. By modeling the diodes with a linear approximation using parameters r_D and V_D, the efficiency of the current-doubler rectifier, considering conduction losses only, is approximated by (21), where r_{LF} represents the

ESR of the filter inductors.

$$\eta_R = \frac{1}{1 + \frac{V_D}{V_{Bat(Max)}} + \frac{\left(r_D + \frac{r_{LF}}{2}\right)I_{Bat(Max)}}{V_{Bat}(Max)}} \tag{21}$$

Additional efficiency improvements can be achieved through synchronous rectification [34]; however, this comes at the cost of increased circuit complexity.

6. Experimental results

An experimental prototype of the four-phase LC_pC_s resonant converter, shown in the graphical abstract, has been built to validate the theoretical proposal. The converter is supplied with a DC-link voltage of $V_{dc} = 400$ V. The power transistors of the inverter stage are Cool MOS™ IPP50R190CE. The heatsinks SK 409/25,4 with $R_{th} = 8.2\ °C/W$ are used for mounting the transistors. The switching frequency is $\omega_p = 2\pi(125$ kHz). The dead time of the transistor driving signals is determined by the IR2111 integrated circuit, with a value of $t_d = 650$ ns. Although a shorter dead time would be preferable to improve circuit efficiency, 650 ns represents a reasonable compromise between efficiency and reliability when using low-cost silicon transistors. According to equation (12), a power factor angle of $\varphi_{zvs} = 29°$ ensures ZVS mode operation for any Ψ value. The maximum charging battery voltage is $V_{Bat(max)} = 53.5$ V. Upon substitution in (14), the transformer's turns ratio is $n = 1$. The maximum current is $I_{Bat(max)} = 10$ A at $\Psi = 0^o$. Considering (18) and using (2), the parallel characteristic impedance is $Z_p = 160\ \Omega$. Finally, from Table 1: $L = 200$ µH and $C_p = 33$ nF. Using equation (15), data collected from datasheets, and experimental evaluation of the passive components with an LCR meter, a first approximation of the parasitic resistance r, responsible for conduction losses, was obtained as $r = 3\ \Omega$. From (15), the approximate efficiency of the resonant inverter stage at full load is $\eta_I = 0.956$. All inductors were constructed using an RM12 core of N97 magnetic material and 16 turns of Litz wire, each consisting of 18 strands with a diameter of 0.315 mm. The gap was adjusted to achieve the desired value of 200 µH with a tolerance lower than 5 %. The resonant circuit capacitors are Metallized Polypropylene Film Capacitors (MKP) from the J series, which specify a 5 % tolerance in their capacitance value.

Limiting the output current ripple, Δi_{Bat}, is essential to prevent battery degradation. The filter inductors used are Vishay IHLP-8787MZ, with $L_o = 75$ µH and $r_{LF} = 30$ mΩ at 25 °C. From (16), the current ripple amplitude in each inductor is $\Delta i_L = 1.945$ A. The r_{Bat} is estimated at 40 mΩ. The output capacitor, C_o, is calculated to achieve a current ripple of 0.1 % of the charging current, $\Delta i_{Bat} = 10$ mA. From (17), $C_o = 1200$ µF. The Schottky diode STPS30M60S, with parameters $V_D = 0.395$ V and $r_D = 0.047\ \Omega$, is mounted on a BOYD 6399BG heatsink with $R_{th} = 3.3\ °C/W$ and used as a rectifier. The transformer is built using an ETD49 core of material N87, with all windings consisting of 16 turns of 42 twisted AWG 32 strands. The series capacitor, $C_s = 68$ nF, is used to dampen the effect of the transformer's leakage inductance on the resonant circuit. The estimated efficiency of the current doubler rectifier using equation (21) is $\eta_R = 0.98$.

6.1. Thermal balancing control results

The control circuit was implemented using a programmable device. The drive signals of each half of the converter and the resonant current waveforms i_2 and i_3 at a full load condition, $\Psi = 0^o$, are shown in Fig. 5 (a). No perceptible current imbalance is observed, with $\widehat{I}_2 = \widehat{I}_3 = 2.75$ A. As the current imbalance between the two sides of the resonant inverter is near its maximum at $\Psi = 90°$, this operating point is selected to evaluate the effect of the current imbalance on temperature. Fig. 5(b) displays the drive signals of each converter half and inductor currents at $\Psi = 90°$. Operation at $\Psi = 90°$ implies that the converter delivers 70 %
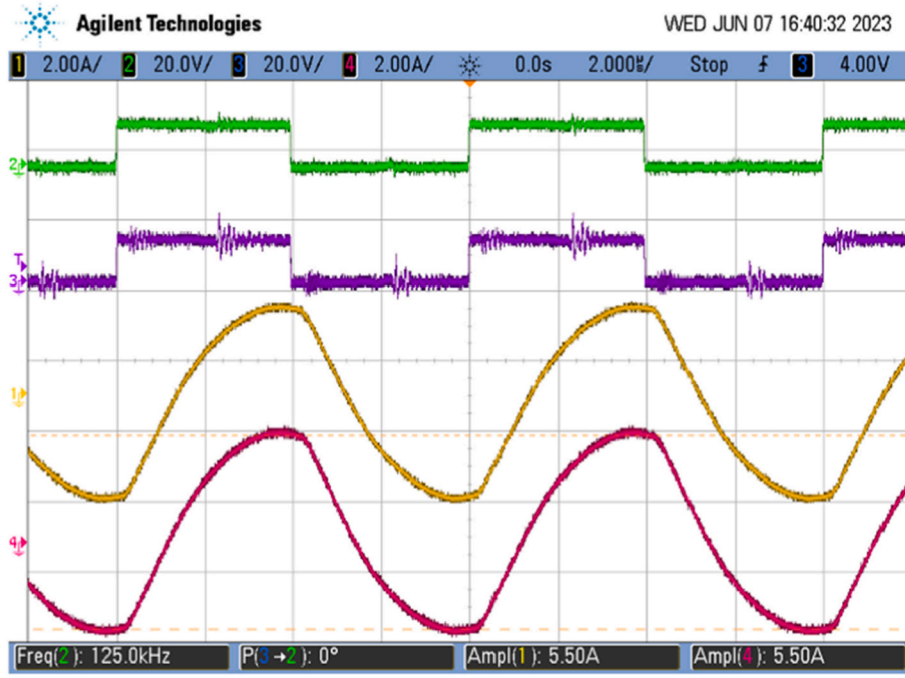
(a)
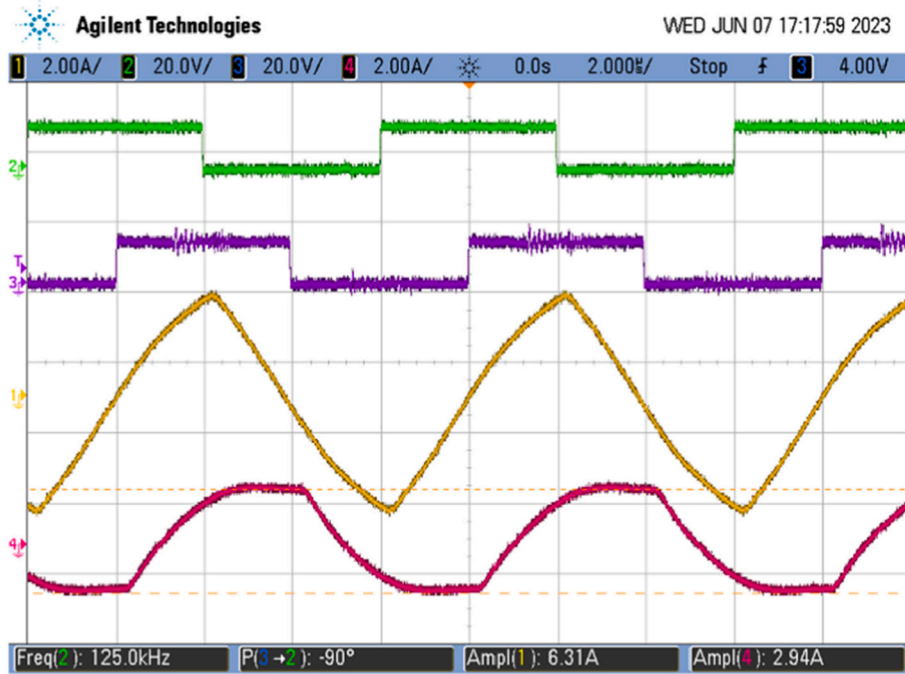
(b)

Fig. 5. (a) Experimental waveforms in the resonant inverter stage at maximum charging current, $\Psi = 0°$. From top to bottom: ch2: Drive signals of transistors M_2 and M_4. ch3: Drive signals of transistors M_6 and M_8. ch1: Resonant current i_3. ch4: Resonant current i_2. (b) Waveforms in the resonant inverter stage at $\Psi = 90°$. From top to bottom: ch2: Drive signals of transistors M_2 and M_4. ch3: Drive signals of transistors M_6 and M_8. ch1: Resonant current i_3. ch4: Resonant current i_2.

of the maximum charging current, as indicated by (2). A significant current imbalance is observed at this point, $\hat{I}_2 = 1.47$ A and $\hat{I}_3 = 3.15$ A.

The thermal transient response without applying the proposed thermal balancing control of inductors $L_{1,2}$ and $L_{3,4}$, which are located on different halves of the inverter, is presented in Fig. 6(a) for a 25 min turn on transient at $\Psi = 90°$. The RMS value of the resonant currents on both sides of the inverter stage, without applying the proposed thermal

balancing control, as a function of Ψ are shown in Fig. 6(b). A significant thermal imbalance is observed, with inductors L_1 and L_2 reaching 102 °C, compared to 55 °C in L_3 and L_4. The temperature difference, $\Delta T = 47$ °C, between the inductors on both sides of the inverter is caused by a current imbalance of $\Delta I = 1.25$ A$_{rms}$, as shown in Fig. 6(b).

The thermal balancing control proposed in Fig. 3(b) was implemented to correct the heavy thermal imbalance. To determine the
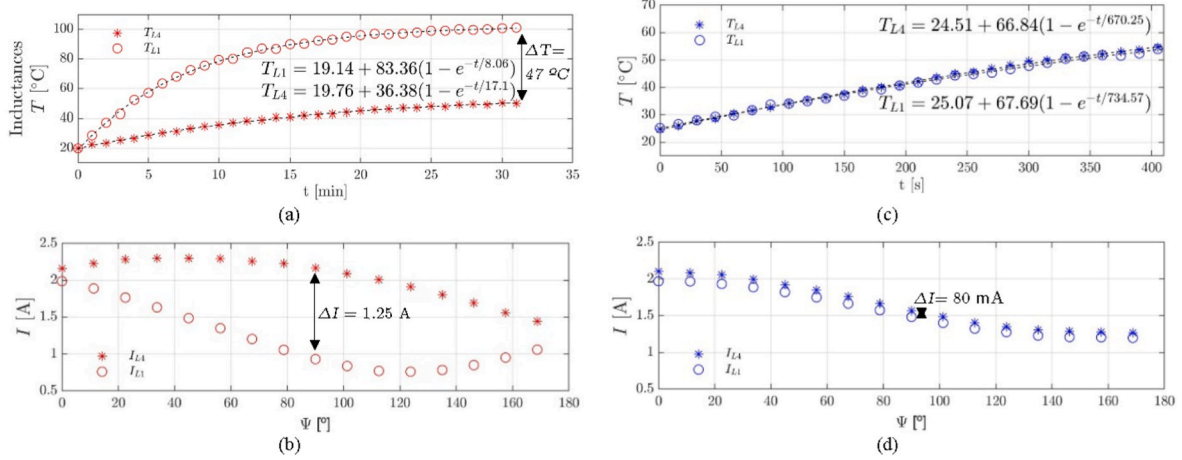
Fig. 6. (a) Measured rms currents through L_2 and L_3 as a function of Ψ without applying the current equalization. (b) Transient thermal response at $\Psi = 90°$ of inductors L_1 and L_4. (c) Measured rms currents through L_2 and L_3 as a function of Ψ after applying the current equalization. (d) Transient thermal response of L_4 and L_1 at $\Psi = 90°$ after applying the thermal balancing control.

winding loss, the ESR of the inductor, r_L, was measured in an HP 4284A LCR meter at 120 kHz with a bias current of 1 A, resulting in $r_L = 0.75\ \Omega$. From (3) and (4), the theoretical value of $\hat{I}_{1,2,3,4}$ was calculated as 2.56 A at $\Psi = 0°$. The winding loss is $P_W = 2.46$ W. The core loss, P_C, was calculated using the Steinmetz equation. According to the N97 magnetic material datasheet, the relative core loss is $P_v = 300$ kW/m³ at 100 kHz, 200 mT, and 100 °C. Given that the volume of the RM12 core is $V_e = 8320$ mm³, the P_C was calculated as $P_C = P_v V_e = 2.5$ W. The total inductor loss is $P_L = P_C + P_W = 5$ W under the given conditions. The closed-form of the thermal response of the inductor, $T_L(t)$, is determined by curve fitting [35] from experimental data of Fig. 6 and matches the step response of a first-order system,

$$T_L(t) = T_A + \Delta T \left(1 - e^{-\frac{t}{\tau_{th}}}\right). \tag{22}$$

The thermal impedance of the inductor is determined with,

$$R_{th}(t) = \frac{T_L(t) - T_A}{P_L} = \frac{\Delta T}{P_L}\left(1 - e^{-\frac{t}{\tau_{th}}}\right), \tag{23}$$

where the thermal resistance is, $R_{tho} = \Delta T/P_L = 15.2$ K/W, the thermal time constant is $\tau_{th} = 474$ s, and the thermal capacitance is $C_{th} = 31.18$ J/K. Temperatures in inductors L_1 and L_4, denoted as $T_{L1,2}$ and $T_{L3,4}$, are measured using the LM35 sensor, which has a 10 mV/°C gain and a typical accuracy of $\pm 1/4$ °C at room temperature and $\pm 3/4$ °C over its full -55 °C to $+150$ °C range. The placement details of the temperature sensors can be observed in the experimental prototype shown in the graphical abstract. The gain of the INA102KP instrumentation amplifier is set to $G = 100$ to obtain a volts-equivalent value of the temperature imbalance $\Delta T = T_{L1,2}\text{-}T_{L3,4}$. The hysteresis band is set to $\Delta T_H = 2$ V, centered around zero, resulting in a reference temperature difference of $\Delta T_{ref} = 0$ V. Under these conditions, the maximum temperature difference between both sides of the converter is $\Delta T = \pm 1$ °C, which is negligible considering the typical operating temperature of approximately 50 °C. A non-inverting Schmitt Trigger comparator implements the hysteresis band, where $R_2 = 10$ kΩ and $R_1 = 2$ kΩ. The exchange of control signals between phases 1–2 and 3–4 is managed by a 2-to-1 multiplexer, whose control input is driven by the thermal management signal, v_T, directly obtained from the Schmitt Trigger comparator.

To validate the proposed thermal balancing control, 28 temperature measurements were recorded at L_1 and L_4 at 15 s intervals. The thermal balancing control ensures precise matching between the temperature

acquired in both halves of the converter, regardless of component tolerances, circuit layout, or parasitic elements, as demonstrated by the results shown in Fig. 6(c). Both halves of the converter operate at the same measured temperature, without any hotspots in the circuit, reaching 52 °C after 6 min. The average temperature difference was 0.77 °C, the maximum deviation with respect to the average was 0.87 °C, and the standard deviation was 0.47 °C. Fig. 6(d) presents the RMS current through inductors L_2 and L_3 as a function of Ψ, following the application of the proposed thermal balancing control. A comparison between the measured current through the resonant branches in Fig. 6 (b) and (d) clearly demonstrates the effectiveness of the thermal balancing control in reducing the current imbalance.

Nevertheless, a small residual difference of approximately 80 mA persists in achieving thermal balance. It is attributed to minor circuit asymmetries caused by component tolerances and layout variations in the prototype. Therefore, the 80 mA current imbalance is a consequence of achieving temperature balance in the presence of non-ideally identical resonant branches.

Fig. 7(a) shows the experimental waveforms of the modulation of the resonant currents' amplitude resulting from applying the thermal balancing control. The envelope of the resonant currents, as shown in Fig. 7(a), is free of oscillations or instabilities, demonstrating a smooth transition between low and high amplitudes and vice versa. Moreover, the battery charging current, $I_{Bat} = 7.2$ A, is disturbance-free. A detailed view of this amplitude modulation is shown in Fig. 7(b), where a smooth oscillation-free transition is evident. The measured settling time is 28 μs, equivalent to three switching periods. The clean transition observed in the current waveforms in Fig. 7(b) is a result of the fast dynamic response of the resonant converter [36], which operates at a switching frequency of $\omega_p = 2\pi(125\ \text{kHz})$ rad/s.

Additionally, the synchronous design of the control circuit enables the exchange of control signals within a single switching period (i.e., 8 μs), as shown in Fig. 7(c). This is achieved by applying a pulse width different from 50 % [37] which minimizes current transients. This perturbation is not propagated to the output, as the rectifier stage is designed to filter out high-frequency switching ripple. Consequently, the thermal balancing control has no impact on the output current.

Battery chargers pose specific design challenges that make them well-suited for evaluating power converter performance, one of which is the wide load variation that occurs throughout the charging process. A PPA5500 N4L Precision Power Analyzer was used to measure the converter's efficiency under thermal balancing control. The efficiencies of the resonant inverter stage and output rectifier were measured separately, as well as the overall efficiency of the prototype. The measured

(a)

(b)

(c)
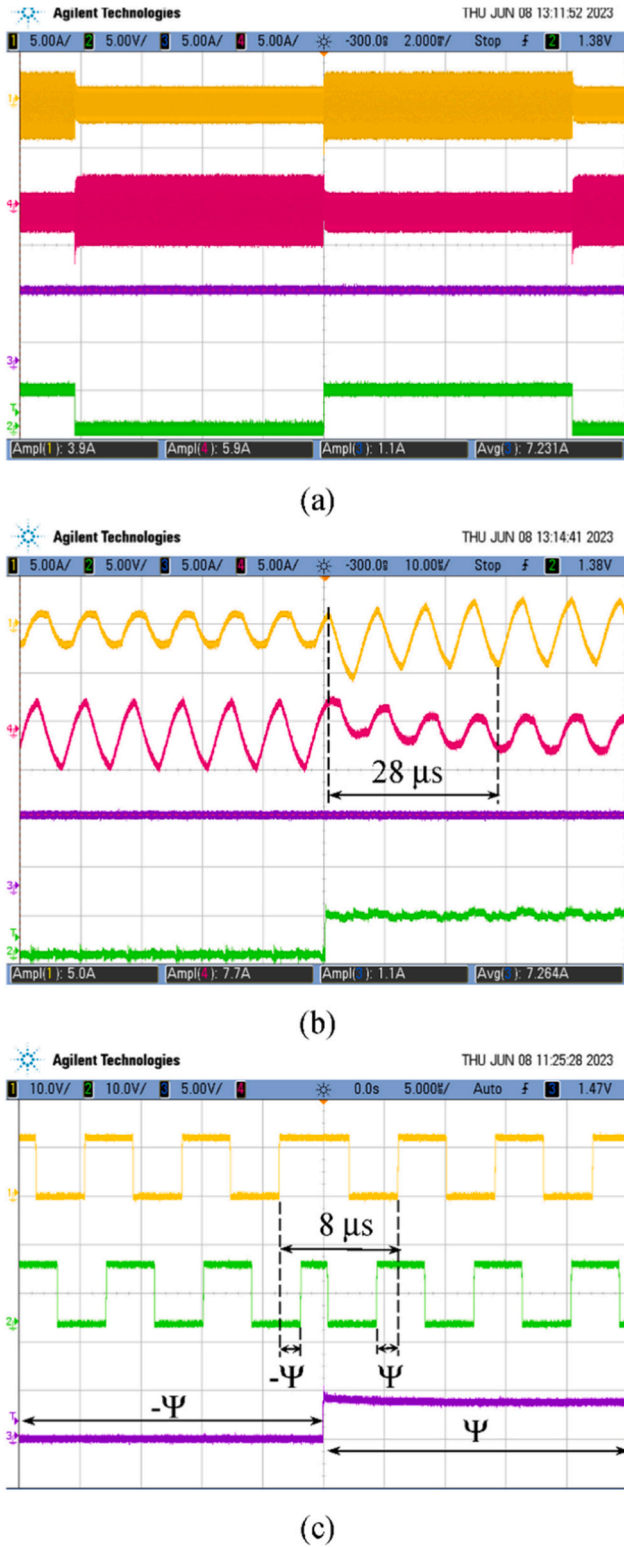
Fig. 7. (a) Experimental waveforms of the converter operating with thermal balancing control at $\Psi = 90°$. From top to bottom: ch1: Resonant current i_2. Ch4: Resonant current i_3. Ch3: Charging current, I_{Bat}. Ch2: Signal command for alternating the drive signals of transistors $M_{1,2,3,4}$ and $M_{5,6,7,8}$. (b) Detail of the amplitude change of the resonant currents at $\Psi = 90°$. From top to bottom: Ch1: Resonant current i_2. Ch4: Resonant current i_3. Ch3: Charging current, I_{Bat}. Ch2: Signal command for alternating the drive signals of transistors $M_{1,2,3,4}$ and $M_{5,6,7,8}$. (c) Details of the drive signal phase transition from Ψ and $-\Psi$. From top to bottom: Ch1: Drive signals of transistors $M_{1,2,3,4}$. Ch2: Drive signals of transistors $M_{5,6,7,8}$. Ch3: Signal command for alternating the drive signals.
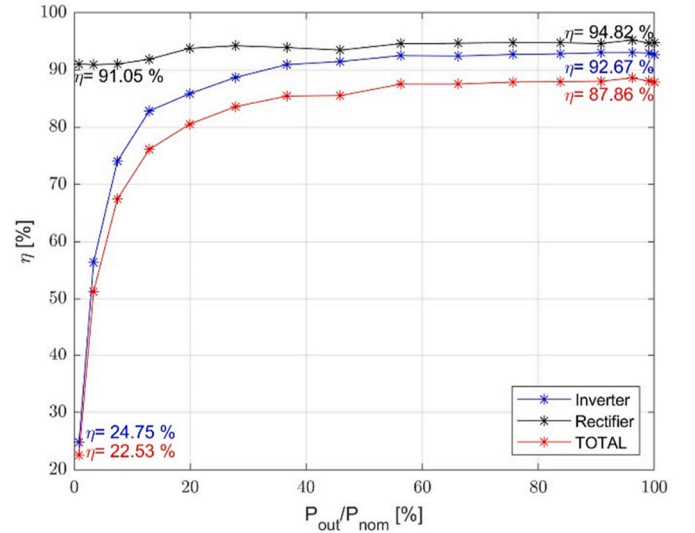
Fig. 8. Measured efficiencies for the experimental prototype. From top to bottom: current-doubler rectifier, the resonant inverter stage and the whole prototype.

efficiencies as a function of the output power are shown in Fig. 8.

The experimentally obtained efficiency value is slightly lower than the theoretical prediction due to unmodeled parasitic resistances, such as those associated with the PCB, cables, and external connection contacts. The prototype's efficiency remains high across a wide range of load variations. Even under light load conditions, such as 20 % of nominal power, the efficiency remains above 80 %, a noteworthy feature of the prototype.

7. Conclusions

Unequal current sharing is an inherent design issue of the phase-shift control in multiphase resonant converters, resulting in thermal imbalance among the circuit components. Observing the symmetric structure of the multiphase resonant converter, it is possible to implement the AM of the resonant currents by exchanging the control signals of the inverter halves without affecting the output current. The resonant current's AM allows the equalization of conduction losses in each converter half to achieve the thermal balance. A thermal balancing control based on a hysteresis controller can correct the possible asymmetries due to component tolerances. The results show the balanced thermal operation of the converter compared to the operation at a constant phase angle. Reducing the temperature of the hottest resonant inductors and semiconductor devices to 25 % is achieved, thereby increasing circuit reliability. Due to the symmetric structure of the circuit, no perturbation at the output is observed. Therefore, the thermal balancing control is fully compatible with the control of the battery charging current. This proposal presents an effective strategy for achieving thermal balance in other symmetrical converter topologies, such as full-bridge, interleaved, and multilevel configurations.

CRediT authorship contribution statement

Christian Brañas: Validation, Methodology, Formal analysis, Conceptualization. **Alberto Pigazo:** Validation, Methodology, Formal analysis. **Rosario Casanueva:** Validation, Methodology. **Francisco J. Azcondo:** Writing – review & editing, Formal analysis. **Francisco J. Diaz:** Writing – review & editing. **Paula Lamo:** Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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