






Review

Hardware-in-the-Loop and Digital Control Techniques Applied to Single-Phase PFC Converters

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Abstract: Power electronic converters for power factor correction (PFC) play a key role in single-phase electrical power systems, ensuring that the line current waveform complies with the applicable standards and grid codes while regulating the DC voltage. Its verification implies significant complexity and cost, since it requires long simulations to verify its behavior, for around hundreds of milliseconds. The development and test of the controller include nominal, abnormal and fault conditions in which the equipment could be damaged. Hardware-in-the-loop (HIL) is a cost-effective technique that allows the power converter to be replaced by a real-time simulation model, avoiding building prototypes in the early stages for the development and validation of the controller. However, the performance-vs-cost trade-off associated with HIL techniques depends on the mathematical models used for replicating the power converter, the load and the electrical grid, as well as the hardware platform chosen to build it, e.g., microprocessor or FPGA, and the required number of channels and I/O types to test the system. This work reviews state-of-the-art HIL techniques and digital control techniques for single-phase PFC converters.

Keywords: power factor corrector; PFC; digital control; converter; Hardware-in-the-loop; HIL



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1. Introduction

Active AC/DC converters ensure that the line current waveform complies with the applicable standards [1] and grid codes while regulating the DC voltage levels [2]. Searching for improvements in efficiency [3], power density and costs results in higher complexity control, involving multidisciplinary knowledge in design, development, testing and manufacturing stages [4].

Diverse alternatives to early prototyping have been used, such as mixed signal simulators [5], simulators with analog and mixed signal extensions [6], or using two simulators at the same time. However, these techniques have long simulation times and their development is complex [7]. Alternatively, Hardware-in-the-loop (HIL) is a technique for performing system-level testing of embedded systems in a comprehensive, cost-effective [8,9], and repeatable manner [10].

The power converter is mathematically modeled and then, a discrete model is implemented in a digital device, e.g., a microprocessor (μ P), Field-Programmable Gate-Array (FPGA) or Application Specific Integrated Circuits (ASIC), which performs a real-time simulation of the power converter, the electrical grid and load. In these simulations, the

digital controller is evaluated as the hardware under test [11] and all the I/O channels, connecting the PFC model and the controller, are at low power levels.

This technique enables a real-time test of the actual controller to be carried out prior to building the plant, so that the simulated parts can be replaced by those already physically implemented as they become available; the test of the controller based on HIL avoids damaging the real plant in extreme situations and the reduction of the development cost, avoiding partial prototyping of the elements of the system and the cost of verification, as well as breakdowns in a real system [12–15]. Beyond that, different electrical and non-electrical systems are emulated on which a control action is validated through the HIL concept [16]. So this can be configured to emulate plants of different applications of electronic systems such as smart grids [17,18] and power converters [19–21], more specifically in PFCs [22,23].

Currently, the HIL implementation is realized with different platforms (e.g., μ P, FPGA, ASIC) [24]. All these systems have common characteristics such as several processors working in parallel; a computer in which the offline model is prepared; input and output terminals interacting with external hardware; and a communication network that allows the exchange of data [25]. The use of FPGAs is preferred because they facilitate the computing parallelization; they allow smaller time-steps [26–28] and the possibility of optimizing the processing speed and area [29,30]. When using fixed point in the models or in the controllers, special attention must be paid to the resolution of the signals involved [7] to avoid the effects of limit cycle, stability problems and a high error in steady state.

HIL has been widely used in electrical power systems with grid-connected power converters [31,32], providing a reliable, economically effective and safe test-bench for development of power converters and their digital controls, within a more decentralized distribution power system scenario which imposes increasing efficiency and functionality requirements. The advantage that HIL brings to PFC controllers is centered on the simulation times that are handled in these systems. Since the PFCs work at the grid frequency, they require quite long simulations, of hundreds of milliseconds, to check dynamics and behaviors of the controller in the transients. PFCs and their controls play a key role in this scenario and are selected as the target for this review. The paper is organized as follows. Section 2 presents common technologies used in HIL. In Section 3, ways to model the converter and how to configure its arithmetic are shown. Section 4 discusses the types of digital control used in this type of application, while, in Section 5, the HIL testing strategies that have been proposed in the literature are analyzed, finishing with conclusions.

2. HIL Technology

In a HIL simulation, the parts digitally simulated in real time totally replace the actual physical components of the system. The Hardware-under-Test (HuT) is tested by connecting it through input and output interfaces (e.g., filters or signal conditioners). It is also possible to execute limited control actions in real time (e.g., opening and closing of switches or disconnection of elements of the system). As is shown in Figure 1a, when the hardware model includes the actual control, it is called a Controller hardware-in-the-loop (CHIL). Since the energy system is virtually emulated, there is no real energy exchange in these systems. This is the paradigm commonly used in the power electronics industry to develop converter controllers that are tested using feedback signals from the controller and generating their own signals that are subsequently sent to the HIL. In the case in which the simulation involves energy transfer (Figure 1b), the system is called Power hardware-in-the-loop (PHIL) [33]. Here, part of the power system is internally emulated and the rest of the system is made up of a real hardware power device externally connected. In this case an energy source (power supply) or sink is needed.

HIL systems have the following characteristics in common [25]:

- i. several processors working in parallel that jointly execute the simulation in real-time;

- ii. a computer in which the offline model is prepared in order to subsequently upload it to the destination platform and monitor the simulation results in real-time;
- iii. input and output terminals to interact with external hardware and
- iv. a communication system that allows the exchange of data between the different blocks that make up the system.

The choice of each element in a smart grid is evaluated in [33] relating them to bandwidth, stability, model accuracy, limitations of smaller time steps, performance and capability limits on actuators and sensors of the interfaces, nonavailability of assessment methodologies, cost and optimization.

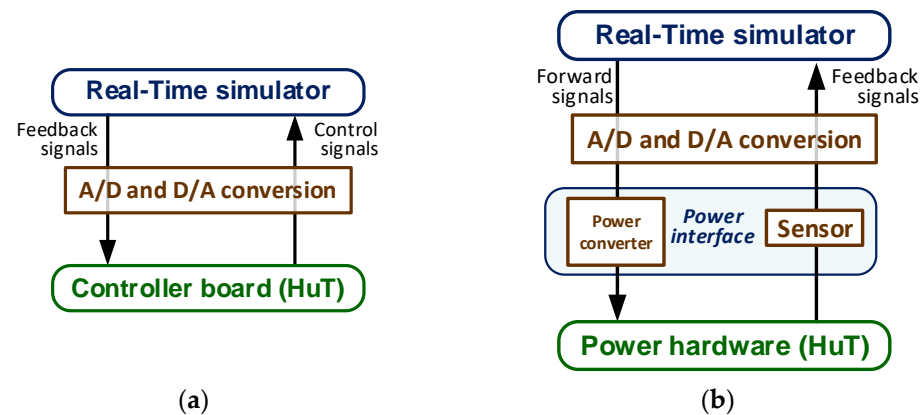


Figure 1. Basic HIL simulation: (a) CHIL and (b) PHIL.

The first HILs were based on the use of computers to carry out the simulations [34]. Its historical and technical evolution in the last 50 years is analyzed in depth in [35].

Despite the above, the use of FPGAs for modeling this type of system makes it necessary to define the arithmetic type used. Determining factors of the system depend on this decision, such as the simulation step, the hardware resources used in the FPGA and the simplicity of design. To simplify this task, high-level tools are available, such as MATLAB or PSIM models, which perform automatic translations into HDL code [34]. In [36], an in-depth analysis of the different software and tools which can be used for the implementation of code in FPGAs in industrial applications, such as those discussed in this work, is made. Another possibility is the use of commercial hardware tools, such as sPHIL [37], Typhoon HIL, dSPACE [38], Opal-RT or RTDS [39], which facilitate the design of the models through graphical interfaces and preconfigured models. In [40], a comparison of the different commercial simulators available is included. These FPGA-based systems use complex models defined by the user without the need for optimization knowledge with small integration steps (around 1 μ s) and PWM input reads of around 10–20 ns. However, they are practically mandatory in complex systems such as [41], where the mitigation of grid harmonics in photovoltaic inverters is studied, or [42], where a fast charger for electric vehicles is tested. In these cases, although the commercial HIL facilitates the realization of the model, the results obtained in terms of consumed resources or integration step are not always optimized [34]. Some companies also offer customized HIL, like Power Smart Control [43].

Commercial HIL

Recently commercial tools have emerged capable of carrying out HIL simulations. HIL is described through schematics, such as electrical simulators. The tool can transform the design of the user into an executable model on a hardware platform from the same manufacturer. These platforms are based on microprocessors, FPGAs or a mixed architecture. Although the equipment runs on an FPGA, it uses an embedded microprocessor to implement the communications and SCADA-type functionalities. In this sense, Typhoon offers its own integrated development environment (IDE) and schematic editor. Other

manufacturers, such as SpeeGoat, Opal-RT [44] or dSPACE [45], use MATLAB/Simulink as their editor. The user uses the Simulink libraries to design the model and, later, that tool of the manufacturer compiles the model that will run in their software.

On the other hand, there are tools that, without being focused on performing HIL, allow some models to be executed in various formats on FPGA-based hardware platforms. NI LabVIEW is a tool based on the graphical programming paradigm called G used by all kinds of instrumentation and control applications and includes SCADA functionality in the tool. NI manufactures its own hardware platforms to augment the technical capabilities of LabVIEW, from data acquisition cards to hardware acceleration platforms. The LabVIEW FPGA functionality allows downloading models or part of them to FPGAs that can be used to create HIL graphical models with the equations of the converter (in other words, it is necessary to write the equations manually) [46]. However, in comparison with the VHDL language, there are limitations, such as time resolution [47]. Another possibility is to use the Real-Time toolbox of MATLAB/Simulink to download models on FPGAs. This option is limited by the number of elements that the toolbox library has but, in return, it allows designs through its schematics or the modeling of the equations in Simulink. In this sense, the company SpeedGoat offers itself as an official partner for HIL from MATLAB/Simulink for its schematics [48].

In [49], a review is made of the main commercial tools in HIL without acquiring a high-cost HIL machine, mainly through evaluation tools. The study analyzes the theoretical characteristics of the tools offered by Typhoon, LabVIEW (comparing “Control Design & Simulation” and “LabVIEW FPGA” tools) and MATLAB/Simulink (comparing “Real Time Desktop” and “Real Time” tools), by observing their specifications and limitations. In the study, Typhoon is shown as the most powerful tool that includes more capabilities from the hardware point of view and its modeling and simulation are more intuitive. LabVIEW offers greater model customization capabilities. While MATLAB has the disadvantage that its “Real Time Desktop” tool simulates inside the processor of the computer that runs it, it does not show use/performance results in specific hardware and “Real Time” needs a physical hardware device to be able to simulate. Table 1 gives a summary of the main characteristics analyzed in [49].

Table 1. Comparative analysis of Typhoon, LabVIEW (“Control Design & Simulation” and “LabVIEW FPGA”) and MATLAB/Simulink (“Real Time Desktop” and “Real Time”) tools, according to [49]. (Reprinted with permission from ref. [49]).

	Typhoon HIL	LabVIEW		Simulink	
		Control Design & Simulation	LabVIEW FPGA	Real Time Desktop	Real Time
Solvers	Exact Trapezoidal Euler	Runge-Kutta 1 (Euler), 2, 3, 4, 23 (variable), 45 (variable) BDF (variable) Adams-Moulton (variable) Rosenbrock (variable) Discrete States Only SDIRK4 (variable) Radau 5, 9, 13 (Variable Order) (variable) Gear’s Method (variable)	The solver used is defined in the logical and mathematical model chosen during the realization of each design.	Discrete (no continuous states) Ode8 (Dormand-Prince) Ode5 (Dormand-Prince) Ode4 (Runge-Kutta) Ode3 (Bogacki-Shampirne) Ode2 (Heun) Ode1 (Euler) Ode14x (extrapolation)	
Data acquisition	Allows data export in various formats during simulation in HIL SCADA (CSV, HDF5, HDF5, MAT, TDMS) HIL402 has built-in oscilloscopes.	Allows to export results directly in Excel or clipboard.	Need other hardware to display the simulated signals.	The data of the different signals can be saved and/or plotted.	

Table 1. Cont.

	Typhoon HIL	LabVIEW		Simulink	
		Control Design & Simulation	LabVIEW FPGA	Real Time Desktop	Real Time
Clock frequency	With the HIL402 hardware virtual machine: 50 MHz	Simulating loops of “Control Design & Simulation” at different frequencies (1 kHz, 1 MHz and in between). Maximum frequency in real time (RT): 1 kHz	MyRIO-1900 Maximum Clock Rate with Zynq-7000 FPGA: 40 MHz	Maximum possible frequency in real time (RT) in normal mode: 1 kHz In external mode: 20 kHz	Depends on the hardware to be used.
Switching frequency	With the HIL402 hardware virtual machine: 200 kHz	The switching frequency shall not be higher than the clock: 1 kHz	Depends on the hardware to be used, but never higher than the clock frequency: 40 MHz	In normal mode: 1 kHz In external mode it is a function of the selected Duty: $f_{SW} = f_{CLK} \times \text{Duty}$	Depends on the hardware to be used.
Minimum simulation step	With HIL402 hardware: 500 ns	1 ms	Depends on the model with a theoretical minimum of 25 ns (40 MHz clock).	In normal mode: 1 ms In external mode: 50 μ s	
Real Time simulation	Works in Real Time on the HIL402 virtual machine.	Simulation at various frequencies (on a PC with 1 kHz clocks or derivatives and with a 1 MHz NI HW or similar), but to be a real real-time simulation, only 1 kHz is allowed with steps or steps of periods of 1 ms.	Realtime on specified NI hardware: myRIO-1900.	In real time at the specified frequencies using the computer’s own processor. In external mode the circuit model is converted to a C/C++ model which implies a higher frequency to simulate.	In real time on the hardware connected to the equipment and linked to the designed model.
Resource utilization/occupied area	Shows summary of HW resources, memory and SW size. Use more high-level built-in resources.	Does not show details.	During the board design, the report shows low-level components (slices, LUTs, DSPs . . .).	Allows analysis of the use of resources.	
Licensing	Free “Typhoon HIL Control Center” software download and registration. Virtual machine with a 1-year license.	LabView 2019 and Multisim 14.2 require a license or the 45-day free trial.	Need the NI myRIO module included with the hardware, and the LabVIEW FPGA payment module.	Simulink Real Time Desktop (not Simulink Real Time) requires license. To make the circuit designs, you need a paid “Simscape Electrical” or a 1-month free trial version.	
Type of simulation	On-line	Off-line	On-line	Off-line	On-line

3. Converter Modeling

HIL implementations rely on precise mathematical models to replicate the power converters, along with hardware platforms, in order to be efficient in real time applications. In this section, proposed mathematical approaches and arithmetic used in the converter operation as well as digital hardware implementations of the HIL are described.

3.1. Mathematical Model

Different mathematical models can be used to describe the behavior of an electronic converter. Although some HIL systems implements an average model of the converter [50,51], the majority of HIL systems use switched models [52]. This is because the switched models are more realistic, as they directly calculate the evolution of every state variable in a small simulation step, being able to reproduce the high frequency events such as the switching noise. Therefore, they are more useful for closed-loop debugging.

The average linearized small signal model [53] consists in linearizing of the system around an operation point. The advantage of this approach is the easy understanding of the system through circuit-based models. But the averaged linear time invariant (LTI) approximation is not accurate enough for PFC applications [54]. As an example, in [22], the converter is modeled via the averaged switch approach because the modeled equations can be solved fast enough within the chosen small time step.

The whole power converter can be modeled with a set of differential equations that, after discretization, result in a state space (SS) model which must be calculated using the values of the state variables in every simulation step [34].

The average model Euler-Lagrange (EL) is used for obtaining the average model, and its converters serve as a basis for obtaining the nonlinear models. In [55], a Lagrangian approach is used to obtain the average model of a Boost converter and is proposed, which recovers, under extreme duty ratio saturation conditions, the individual EL formulations of the intervening topologies of the circuit. In [56], the average Boost converter circuit is also written by EL equations.

The Hamiltonian modeling encompasses the Lagrangian and represents the systems as interconnection ports, where the product of the port variables is the power, that is the rate of change of energy [57]. The state variables are those related to energy store elements, such as capacitors and inductors. Despite having specific mathematical and physical interpretations, Port—Controlled Hamiltonian (PCH) model can be obtained by EL model and both are mathematically similar to the models described in state space. An example of application of the Euler-Lagrange, state space and PCH models is shown in [58].

In [23], the model of the PFC stage is reached by dividing the circuit into a linear part, using a state space representation based on the Padé approximant and a nonlinear part, given by a switch state dependent feedback.

Table 2 summarizes the main specifications of the proposed HILs which use different mathematical approaches to comply with reliable models of converters. Moreover, contrast experiments to validate the suitability of these models and their implementation in different platforms are also highlighted.

Table 2. Specifications of the proposed HILs.

Proposal	Mathematical Model	Converter	Experimental Verification	Platform
[47]	LTI + State Space	LLC resonant	PSIM	FPGA
[24]	Average switch approach	AC-DC PFC	MATLAB/Simulink (CHIL simulation)	PC
[34]	State space/Euler Lagrange	Buck	LT3430-1/LTC3892-1/MAX1685	FPGA
[50]	Euler-Lagrange	Boost, Buck and SEPIC	MATLAB/Simulink (Real plant)	DSP
[25]	Padé approximation with oversampling	Rectifier PFC	MATLAB/Simulation (Real plant)	FPGA

3.2. Arithmetical Possibilities

The election of the mathematical model must be associated with the choice of the arithmetic to be used in the HIL model. The latter is responsible for defining key HIL parameters, such as its size, e.g., memory or area requirements, or the minimum simulation step, i.e., time resolution. The choice of the arithmetic depends on the target used for the implementation (μ P, FPGA, . . .) but also the abstraction level and development tools due to the language used must be considered (VHDL, C, Verilog, . . .). For example, in [34], the following VHDL classification is presented:

1. Real Arithmetic: this is the standard numeric type that uses double-precision floating-point format. It cannot be synthesized, but it is useful to create a first approximation.
2. Float Arithmetic: this is a synthesizable floating-point arithmetic. It has the versatility of floating point, but it needs many hardware resources.
3. Fixed Arithmetic: this is a fixed-point arithmetic. The designer must decide the number of bits to the integer and the fractional parts of every variable, and it needs much more design effort.

Floating point arithmetic is easier to use and translating equations from the mathematical model to code is straightforward in most cases. An example of this application is shown in [59] where the DCDC converter was described with single precision floating point arithmetic with a state-space approach and two states. In cases where the simulation step is critical, the fixed point is more interesting. In [7], a power converter is modeled using different arithmetic and it is evidenced that the use of a fixed point increases the processing speed and decreases the number of hardware resources used. This same result is shown in Table 3, where an addition and subtraction operation are synthesized using two numbers in fixed point and in floating point using xc7a100t-csg324-1 FPGA in Xilinx Vivado, where the timing is nine times faster in the case of 32-bits integer than with 32-bit floating point [60]. On the other hand, some platforms allow configuring the resources consumed in an operation to adapt to the needs of the system. Table 4 shows an example of how it is possible to define different resource settings and delay times in the same operation using a multiplication of two floating point numbers employing xc7a100t-csg324-1 FPGA in Xilinx Vivado.

Although synthesis tools have evolved enormously in recent years and these differences have been diminishing with new tools, these differences still exist. However, it cannot be the only element to consider when choosing arithmetic since using fixed point in complex converter models can involve a significant design effort that may not be attractive [34]. With the use of fixed point, it is necessary to define in each stage the location of the point that will be fixed according to the range of values that the variable takes and it will be necessary to modify it with each reconfiguration proposed.

Table 3. Summary of the hardware resources and timing in an FPGA by performing addition and multiplication operations with two 32-bit numbers using fixed point and floating point (int32 and float32, respectively).

Operation	DSP48E	LUT	Timing
$float32 \times float32$	3	135	52.435 ns
$float32 + float32$	2	195	88.970 ns
$int32 \times int32$	4	231	19.315 ns
$int32 + int32$	0	186	4.658 ns

DSP48E and LUT are digital signal processing logic and Look Up Table elements, respectively.

Table 4. Summary of the hardware resources and timing in an FPGA by performing multiplication operations with two floating point numbers.

Operation	DSP48E	LUT	Timing
$float32 \times float32$	0	675	78.780 ns
$float32 \times float32$	1	267	67.505 ns
$float32 \times float32$	2	122	54.690 ns
$float32 \times float32$	3	135	52.435 ns

4. Test

Testing controllers for power converters using HIL are gaining acceptance. Recent proposals include the following representative examples:

- Statistical tests [61], such as the Monte Carlo method, that require multiple iterations to simulate failure cases.
- Low-cost multi-solver real-time simulation environment [62], namely the real-time extension of the virtual test bed (VTB-RT). In this proposal, for a given hardware platform, the minimum time resolution is limited and only a limited bandwidth of the system under test can be used. So it is necessary to pay attention to the compromise between the VTB-RT platform cost and the bandwidth of the system under test.
- Reconfigurable HIL based on a top-down design flow [63] analyzed through a fault-tolerant shunt active power filter application. In [64], it is also shown how HIL devices are used to assist in the design, optimization and quality assurance of controllers from the early design stage all the way to the type testing and release testing stage.
- HIL for the validation, in the time and frequency domains, of the input and output impedances of converters achieving ultra-low latency in real time [65]. This work also shows a comparison between real-time emulation and a reference hardware design under steady-state and transient conditions.

5. Digital Control

The difference between the response obtained when the controller interacts with the HIL and the actual converter is caused by the latency between the signals sent by the controller and the output of the HIL. The total latency must be kept to a minimum by using a very small-time interval during the simulation [66].

Generally, the control in PFC is done with two loops: an internal and fast current loop to achieve near unity power factor, and an external and slow voltage loop to stabilize the output voltage. In this case, usually three variables are necessary: input and output voltage (v_{in} and v_{out} , respectively), and input current (i_{in}), although there are other proposals in the literature, as in [67–69], that eliminate the need to use the current sensor.

According to [70], current control techniques classify the digital control of the PFCs into four groups (Figure 2):

1. Group I: Operation in discontinuous conduction mode (DCM) or the boundary condition between the continuous conduction mode (CCM) and DCM (Figure 2a).
2. Group II: Non-linear carrier (NLC) control of the line current, where the switching instants are identified by the comparison of the current with a carrier signal, hysteresis

- band or a sliding surface that imposes the proportionality between the peak, valley, or average current and the input voltage in each switching period (Figure 2b).
3. Group III: Linear control of the average current. Noise immunity improves compared to the NLC technique at the expense of reducing the bandwidth of the current control (Figure 2c).
 4. Group IV: Phasor-based control. The input voltage is assumed to be sinusoidal, so the modulation function that imposes the line current must be sinusoidal (Figure 2d).

As an example of Group I, in [71], the operation characteristics, the modeling and the control system of the DC-DC SEPIC PFC converter in CCM and DCM are presented. The authors compare two different controllers and finally, they suggest a new nonlinear controller called Adaptive Passivity-Based Feedback Linearization Control.

The non-linear control, Group II, is the best adapted to the different operating points of a non-linear and time-varying system such as the converter. In its original version it is implemented with a simple comparator (in its average version, the complexity does not increase substantially). These attributes make it a very interesting option to leverage the digital circuit capabilities, improving the noise immunity and including predictive algorithms. One example of this is [56], where the non-linear control of a boost converter PFC and SEPIC converter is tested; while, in [72], nonlinear control techniques applied to static power converters are implemented and compared in HIL: State Feedback Linearization (SFL), passivity Based Control (PBC), and Interconnection and Damping Assignment Passivity Based Control (IDA-PBC). Here, each model is associated with a control technique. The EL model is the base model for the others. The Euler-Lagrange model is associated with PBC control equations, SFL control uses the model description in state space (SS), and the IDA-PBC control requires the PCH system.

Group III controls present the following advantages:

1. Its bandwidth of the current acquisition stage is smaller than in the non-linear version.
2. In bidirectional PFCs, the non-linear control may exhibit non-stable operating conditions.

It has better immunity to high frequency noise due to its lower bandwidth (both sensor and control loop), as well as acquisition techniques (synchronization between acquisition and switching).

An example of the Group IV technique, based on the introduction of sinusoidal input voltage, gaining immunity to grid disturbances, is shown in [73] where a traditional linear control with two loops is proposed for a bridgeless SEPIC PFC converter. In [74], the proposed control is based on a multi-thread software structure where time critical tasks are performed in a fast interrupt service routine, repeated every switching cycle in a totem pole PFC. Appropriate control measures are employed to address current spikes during zero crossings and AC voltage drop handling issues.

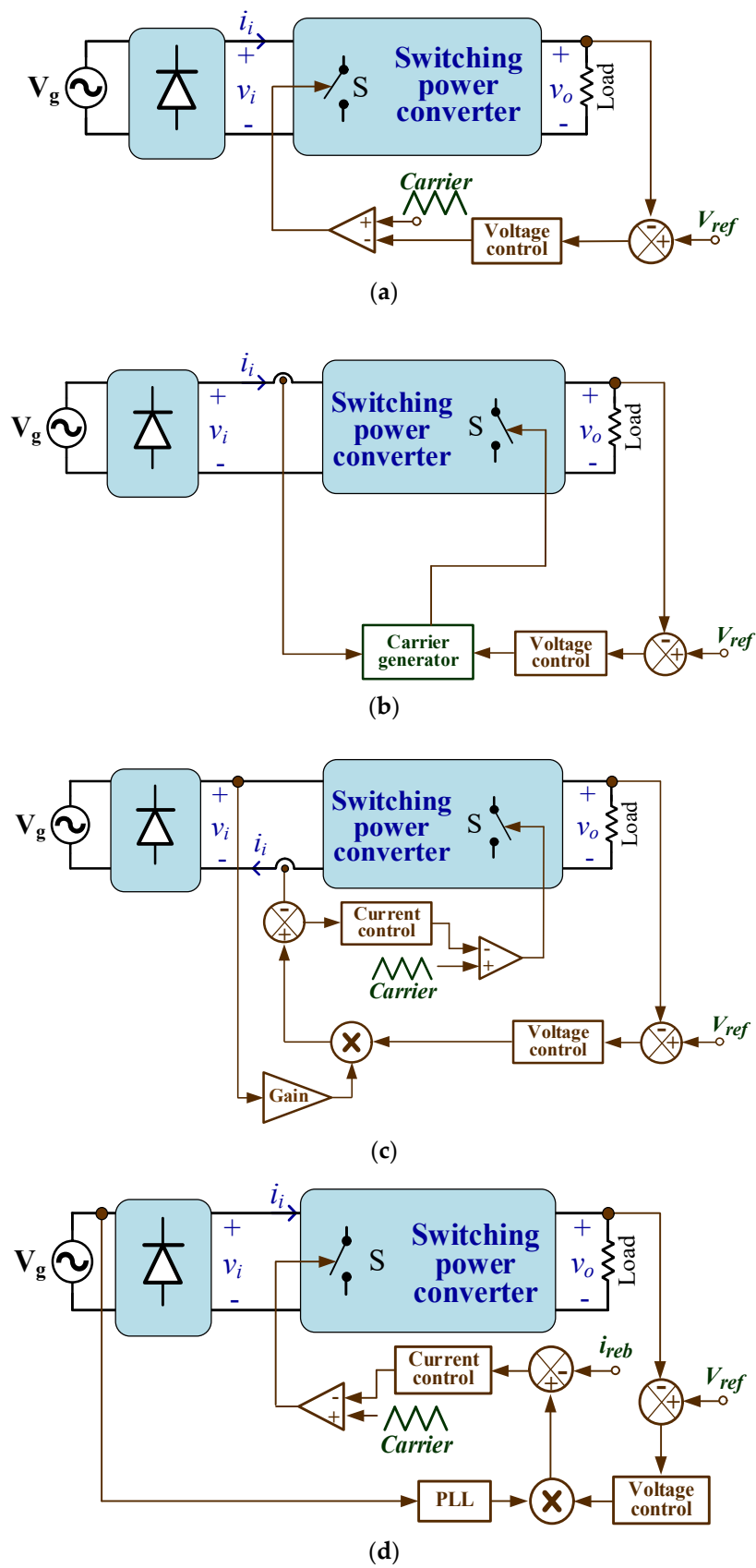


Figure 2. Types of current control techniques in PFCs. (a) Group I, (b) Group II, (c) Group III and (d) Group IV.

In [75], the contributions of FPGAs to the control of industrial systems, including power electronic converters, are presented, establishing three main design rules that focus on the algorithm refinement, the modularity, and the systematic search for the best compromise between the control performance and the architectural constraints. Another common option is to find the use of FPGAs together with processors [35] where the FPGA carries out sampling and conditioning tasks of input and output signals in parallel to the processor. Examples of this type of system are dSPACE and Opal-RT [35].

PWM

The pulse width modulator (PWM) is the block that samples the output signal of the controller. In a first approximation to this block (Figure 3a), which corresponds to natural sampling, the generation of PWM comes from the comparison of the modulating signals, resulting from the control action, v_c , and a linear function, the carrier, in the period of switching. When a digital controller generates the control signal there is a double digitization (Figure 3b) where the signal v_c^* is the output signal of the digital controller, whose update period depends on the clock of the digital circuit, and v_{cT}^* , which is the control signal sampled by the PWM block. If uniform sampling is adopted, the value of v_c^* is taken at the beginning of each switching period to obtain the PWM signal (Figure 3c), avoiding the occurrence of a vertical crossing [76].

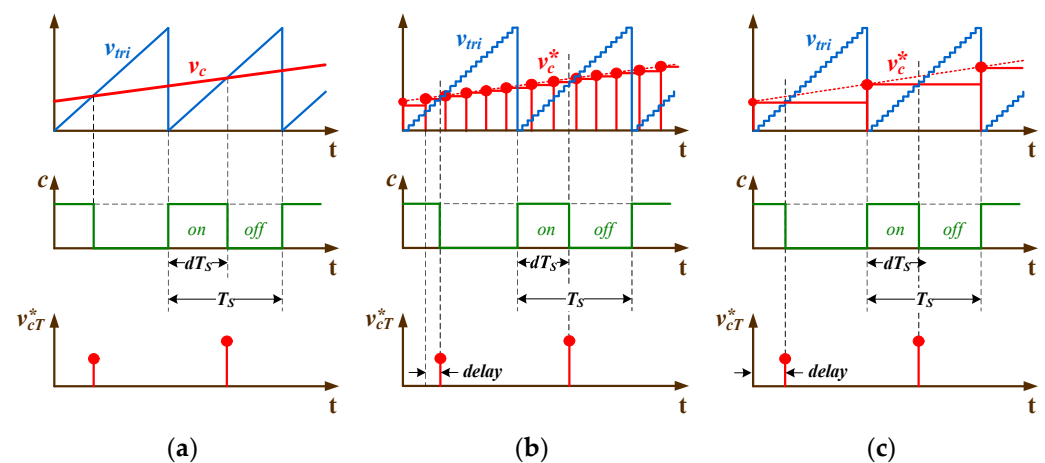


Figure 3. PWM modulator with trailing edge sawtooth carrier signal. (a) Natural sampling, (b) double sampling of the control signal, and (c) sampling of the control signal at the beginning of each switching period.

This comparison of the two signals generates a logic 0 and 1 output signal, indicating the off and on state of the switch respectively. The resolution of the PWM depends on the number of clock cycles in the switching period and the type of carrier. In [77], how to increase the resolution of the PWM block is presented, oriented to prevent one of the limit cycle conditions.

The literature shows examples of PWM that use from a minimum of 20 samples per PWM period [59] to hundreds [64] or even thousands [78]. In addition, it is possible to synthesize different types of digital pulse width modulators, depending on the relationship between the sampling frequency and the switching frequency and different carrier waveforms [79], and use numerically different PWM sampling and simulation steps (for example, in the commercial tool Typhoon HIL602 the PWM sampling step is 20 ns, and the simulation step is reduced to 500 ns [80]).

Control and carrier signals are both the elements under the test carried out by interacting with the HIL and are finally implemented in the real system. Their implementation is therefore not a model, but the actual design. It is common to adopt the switching period as the sampling period for the controller, which introduces a known error and time delay in comparison with the analog counterpart, so design constraints to limit those effects

are introduced. However, the carrier signal of the PWM block or the NLC has the largest resolution, allowed by the digital implementation of the controller in the actual converter, because this resolution defines the achievable step change of the power variables, i.e., current and voltage. On the other hand, the higher the time resolution of the platform that allocates the HIL, the closer are the results achieved to the actual converter response. FPGAs are preferred to develop HIL projects because of their capability of defining concurrent digital blocks, and thus make the most of the clock time resolution.

6. Conclusions

This manuscript provides an overview of HIL and digital control techniques applicable to single-phase PFCs. Initial verification stages in early PFC prototypes are avoided through HIL, which reduces the product time to market and the development costs.

After introducing HIL and approaches used for PFC design and validation, an overview of the available customized and more general tools is also given. From a user perspective, the main differences rely on the maximum accuracy and resolution achieved in each case and, generally speaking, customized tools result in better resolutions by selecting the most suitable target, mathematical model and solver for each application. However, more generalist tools provide a better integration with other tools required during the design, or the final verification stages. The modelisation of the power converter is also a key point to achieve the required accuracy and time resolution. State space, average and switch, and Euler-Lagrange approaches are commonly used in HILs for PFCs. However, not only is the mathematical model relevant, but also the selected target for the HIL. The most commonly used target for HIL in PFCs is FPGAs, which allows the best time resolution among the available targets.

The choice of technology and model to use for the development of a HIL depends on the type of application and the available budget. To make a low-cost version, the designer can use tools such as spHIL, which include a very intuitive graphical interface to configure the pre-designed models and use an inexpensive FPGA (over 100 euros). However, if it is necessary to design an ad-hoc model not included in a commercial product, an economical solution is to design a custom model and implement it in an FPGA using VHDL language, or use a NI myRIO device and design the HIL model using a graphical language in LabView. Following Table 1, the latter limits the HIL capabilities but gains in flexibility. When requiring higher performance, it is necessary to use a specific commercial system for HIL, such as Typhoon HIL, dSpace or Opal-RT. These systems are scalable and the design procedure of the HIL is carried out through the schematic of the power stage in a very patterned way. However, the cost of this type of system is high (over several thousand euros).

The digital controller receives inputs from the HIL and generates the switch-gate signals. This implies that the HIL complexity, hardware resources in terms of both A/D and D/A interfaces and processing capability should be adapted to the type of used controller. Moreover, certain control techniques, such as current rebuilding, involve a high time resolution, which also affects the decision about the mathematical model, solver and selected target for HIL.

All in all, mathematical models, solvers, targets and digital controllers must be balanced to speed up the verification stage of the power converter and its controller. These proposals can be developed through more general high-level techniques, which are fast and consume large hardware resources, or through ad hoc designs in which the designer must specify the mathematical model, arithmetic and technology to be used based on their needs.

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